

FIG. 1B

2022-26-30 00:00:00

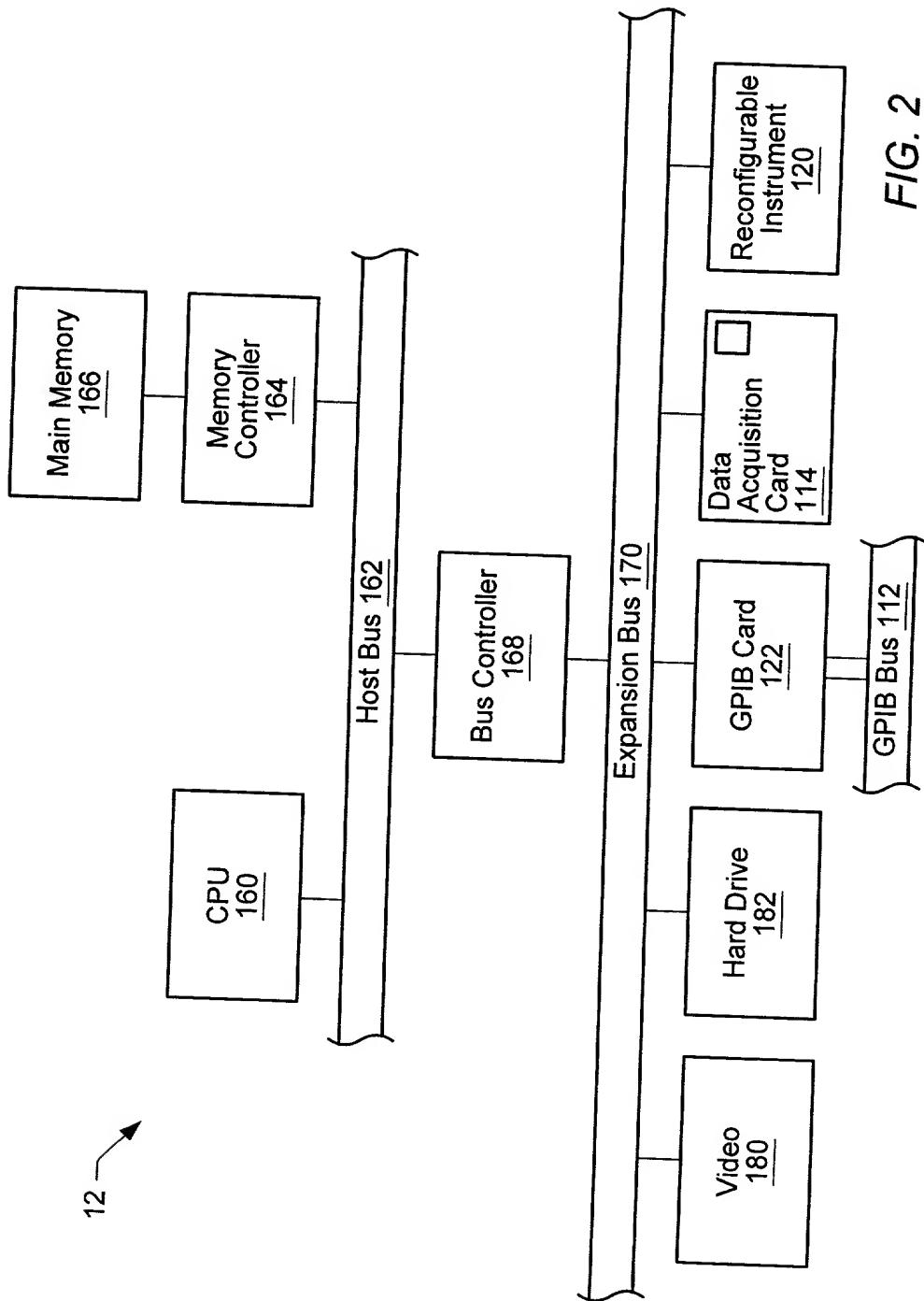


FIG. 2

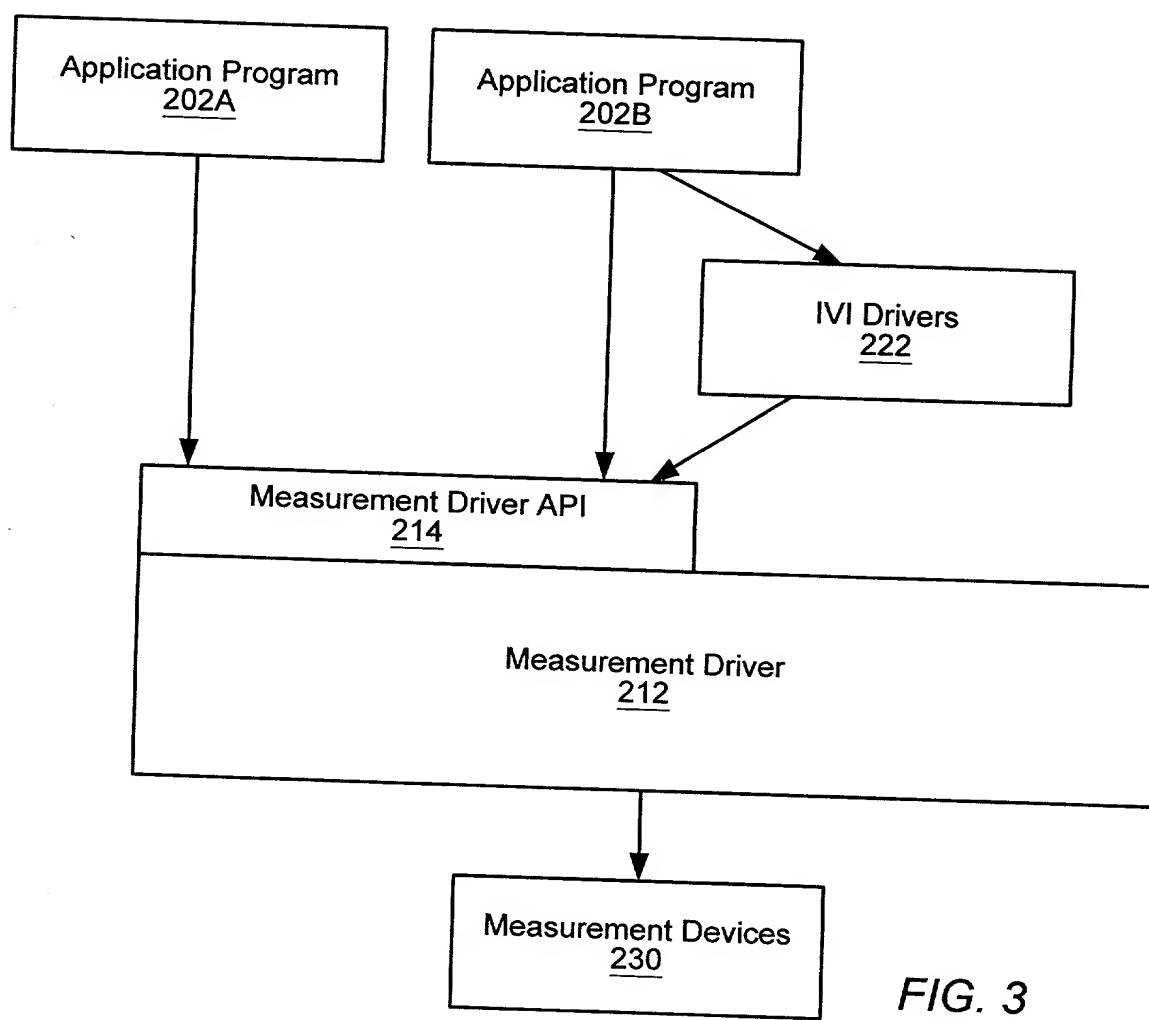


FIG. 3

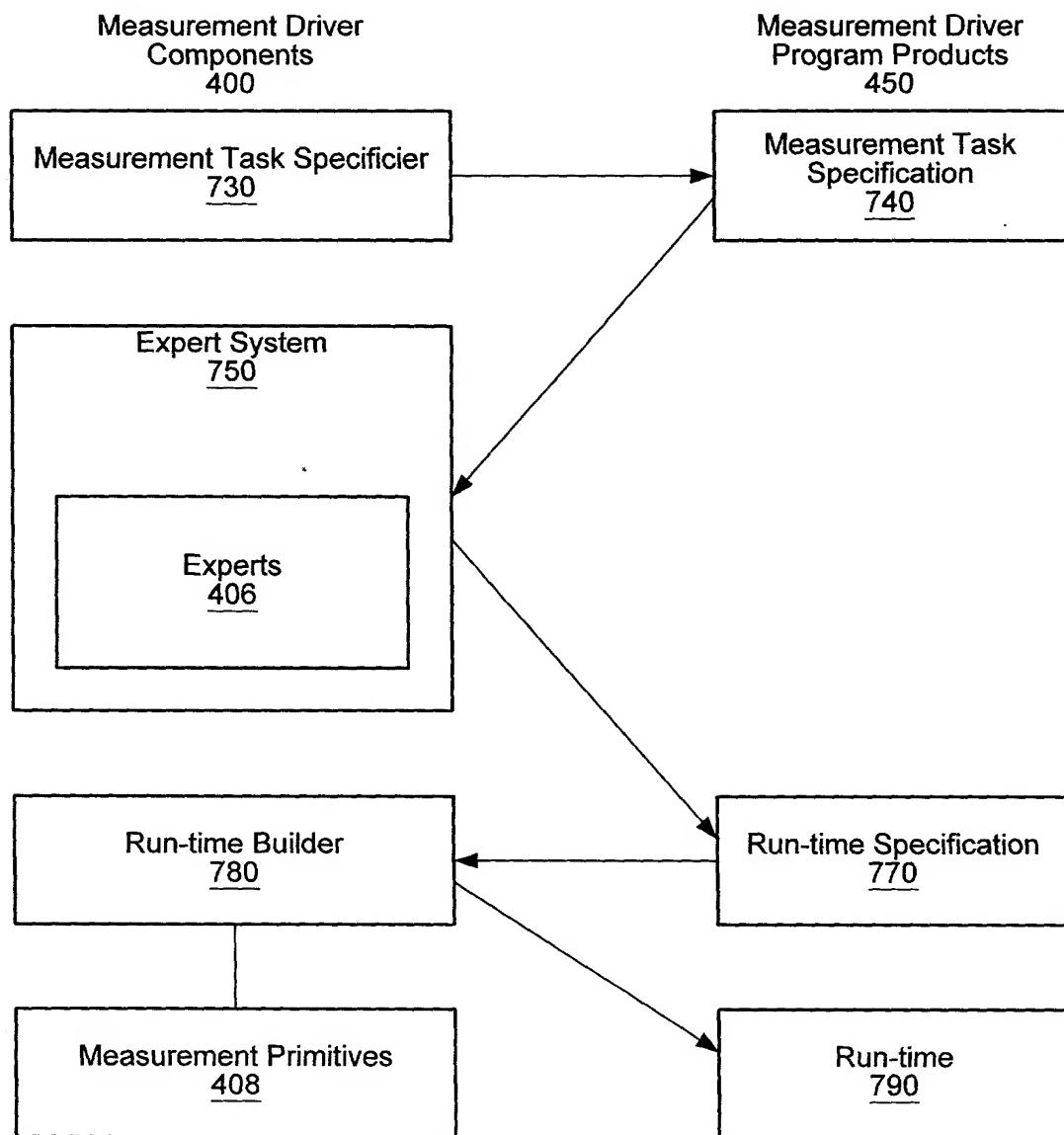
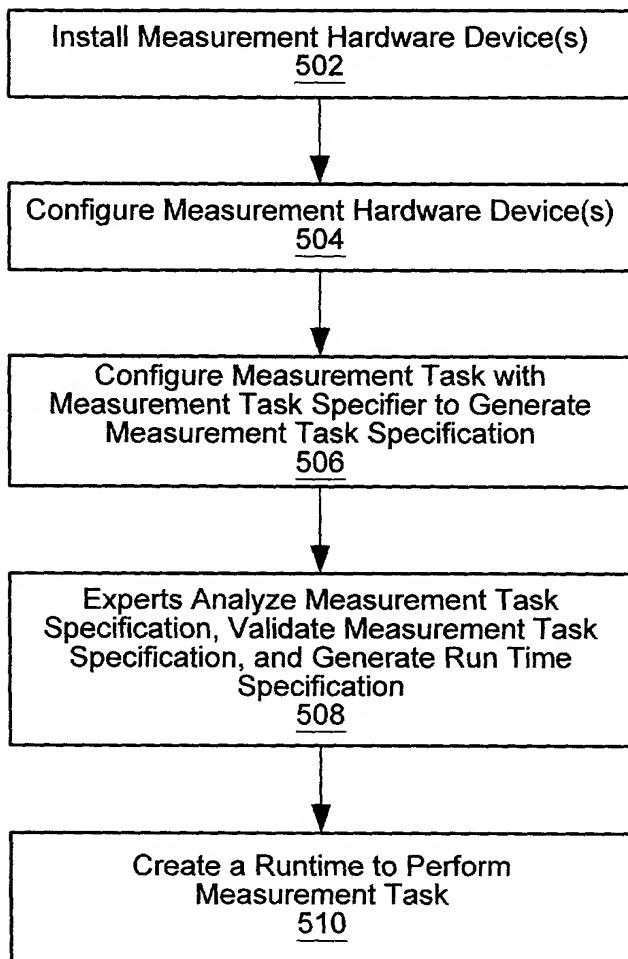


FIG. 4



*FIG. 5*

2022-26x3000.tif

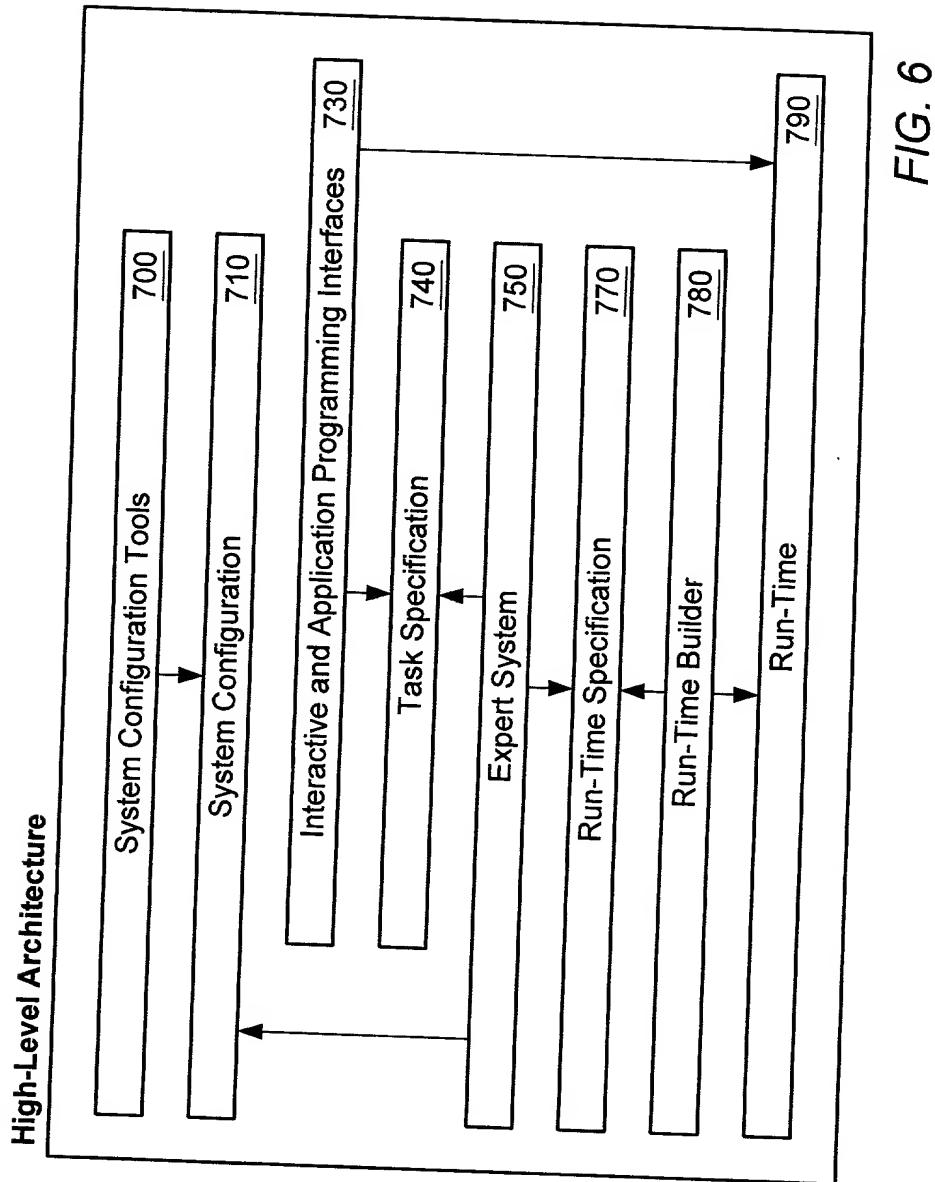


FIG. 6

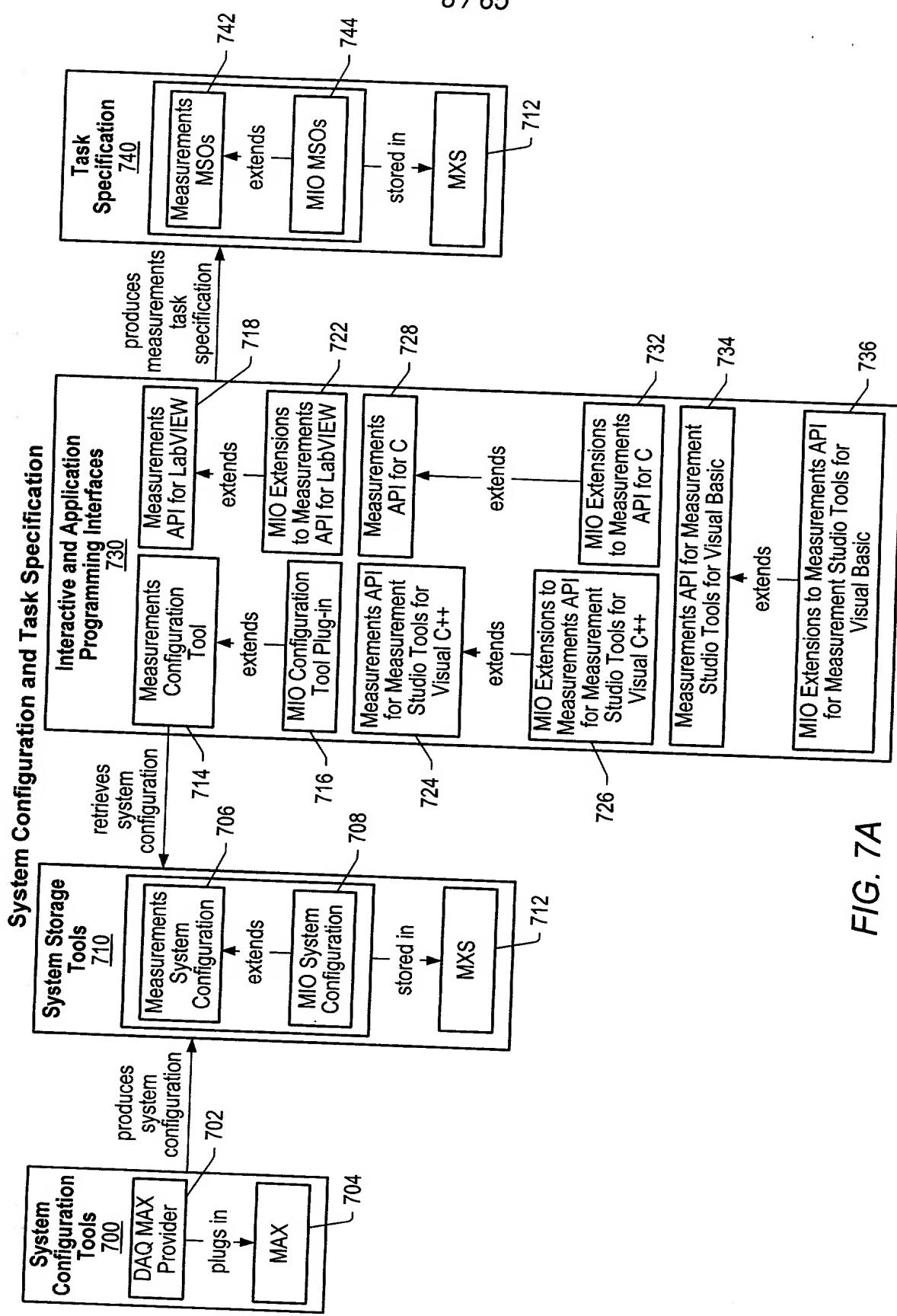


FIG. 7A

## Compiling Task Specification to Task Run-time Specification

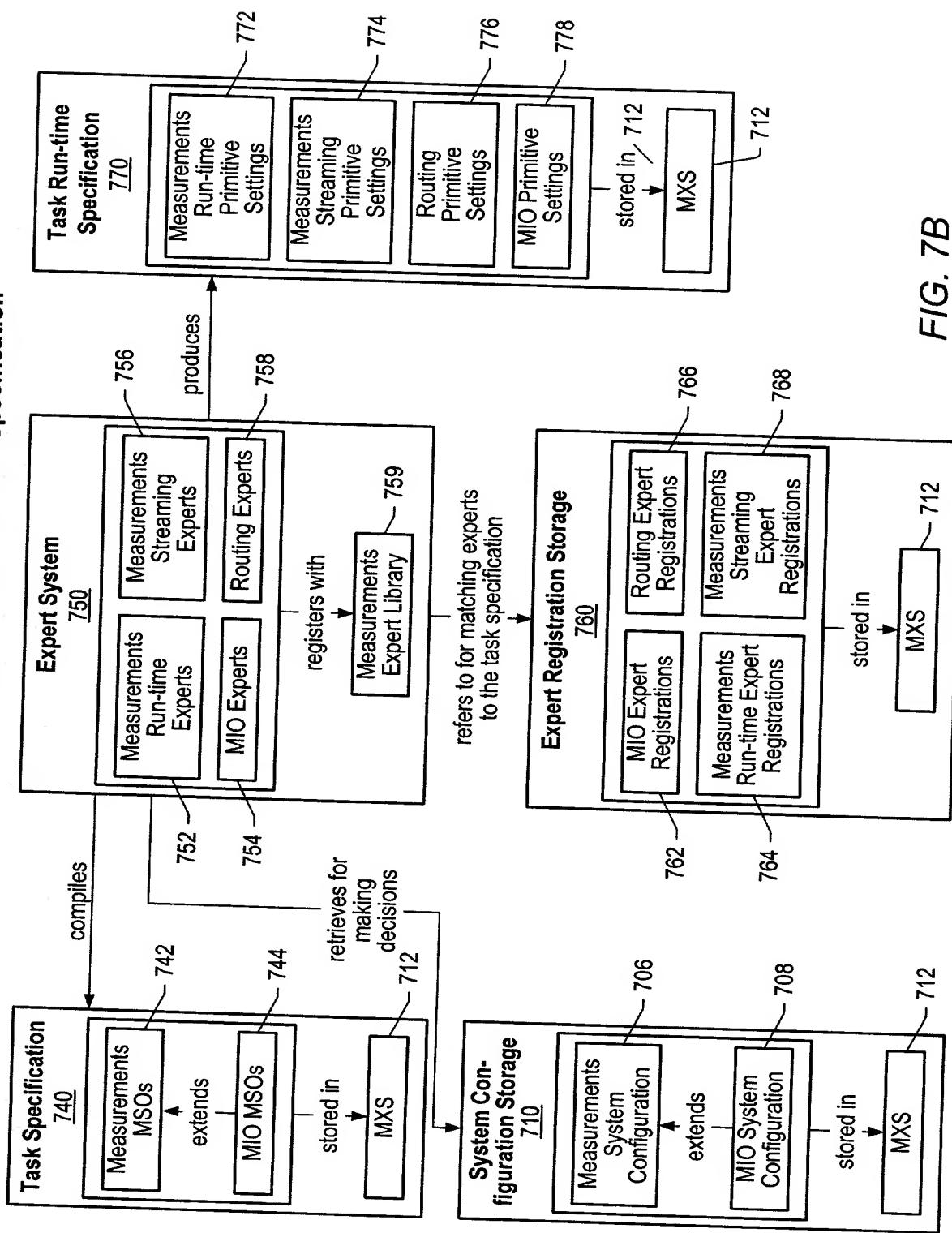


FIG. 7B

### Building Task Run-time from Task Run-time Specification

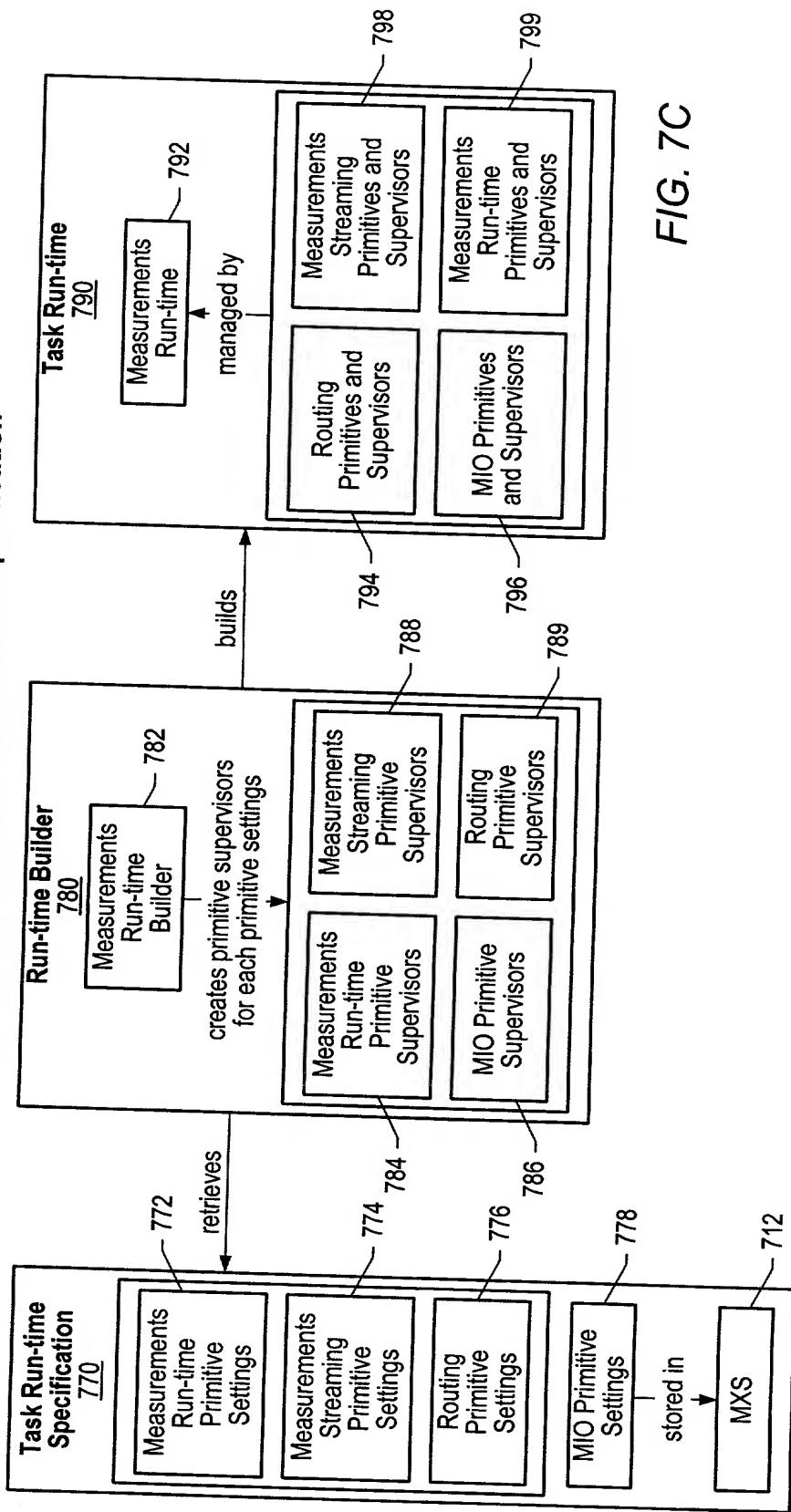


FIG. 7C

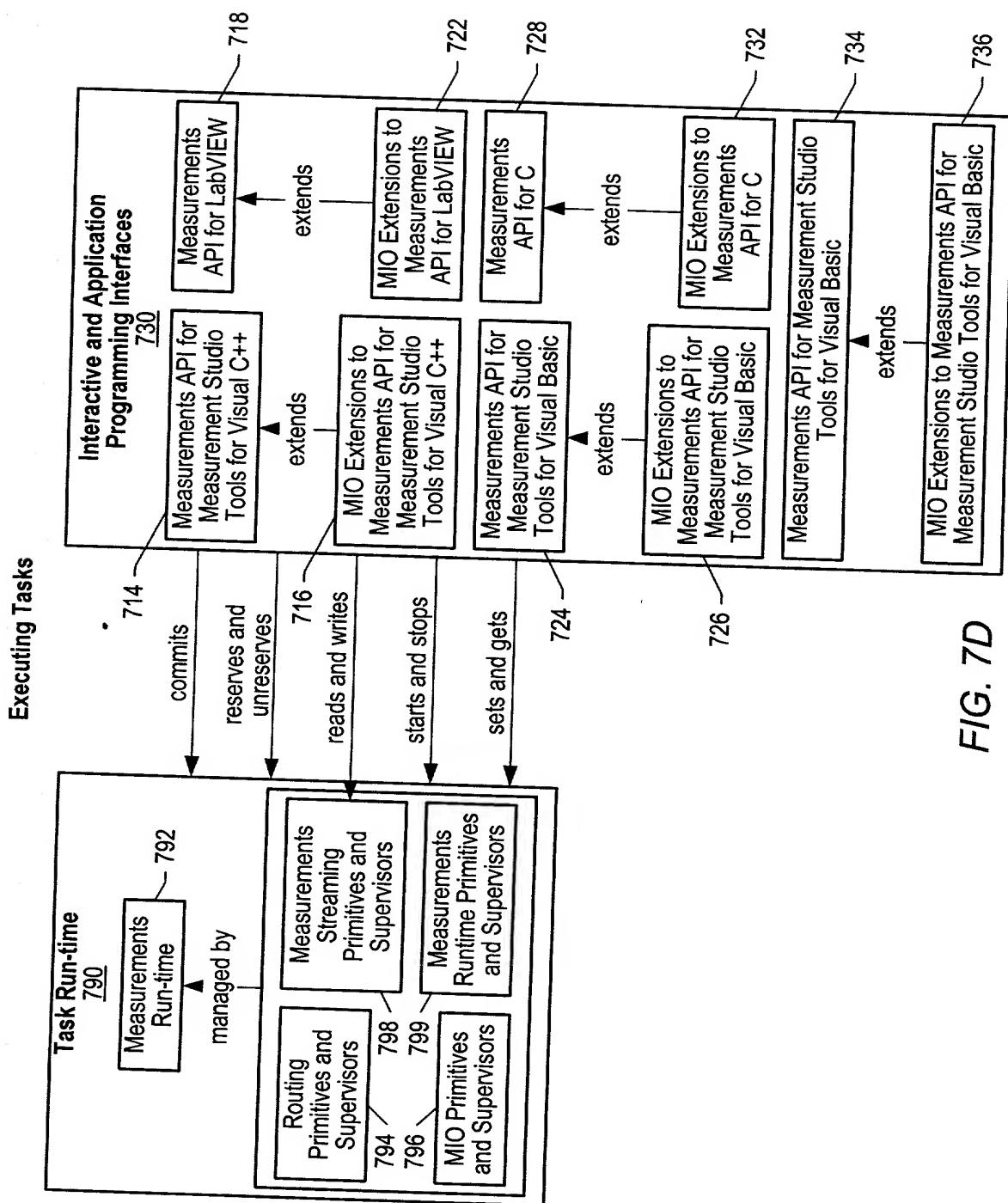


FIG. 7D

**Packages for System Configuration and Task Specification**

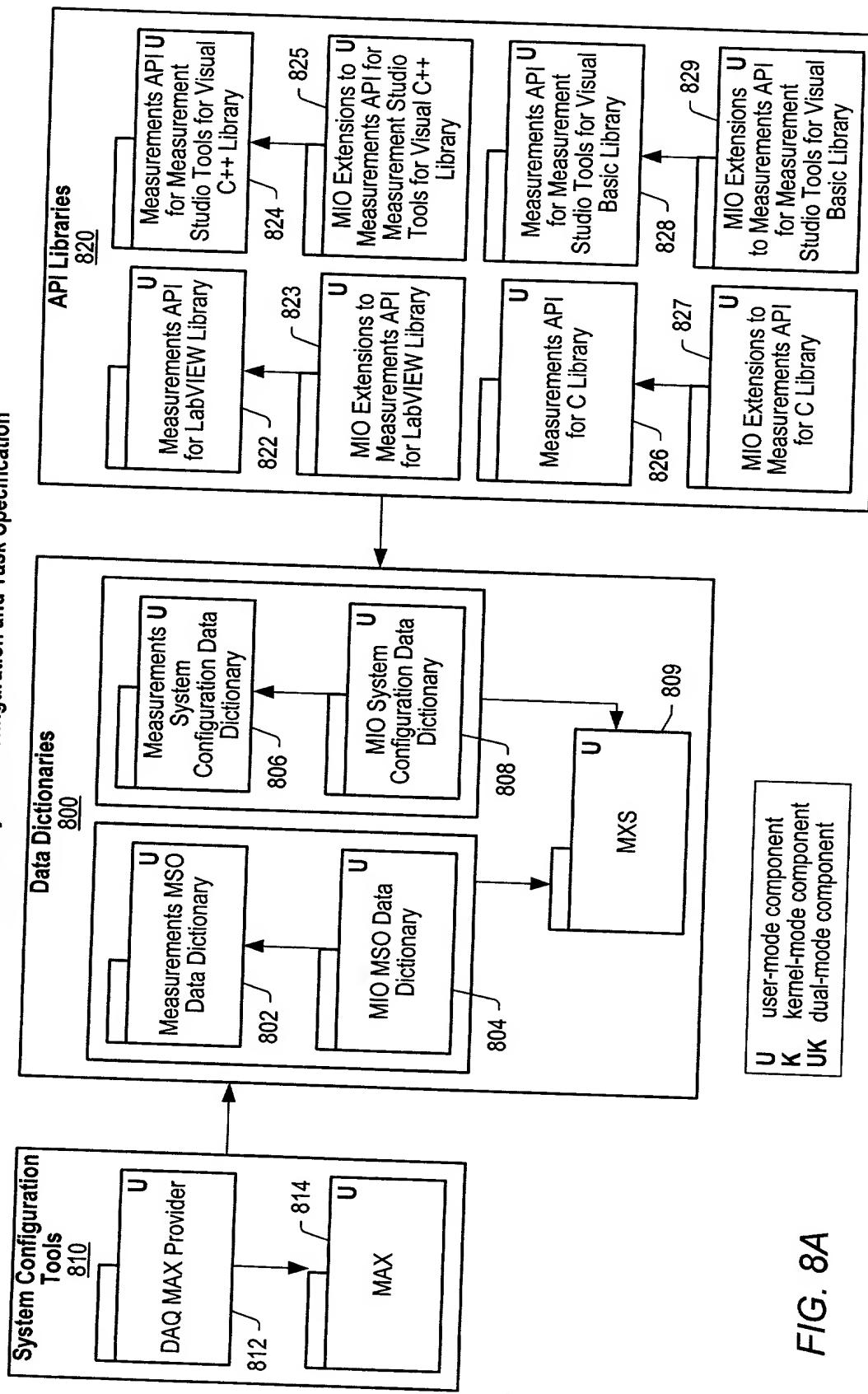


FIG. 8A

## Packages for Compiling Task Specification to Run-time Specification

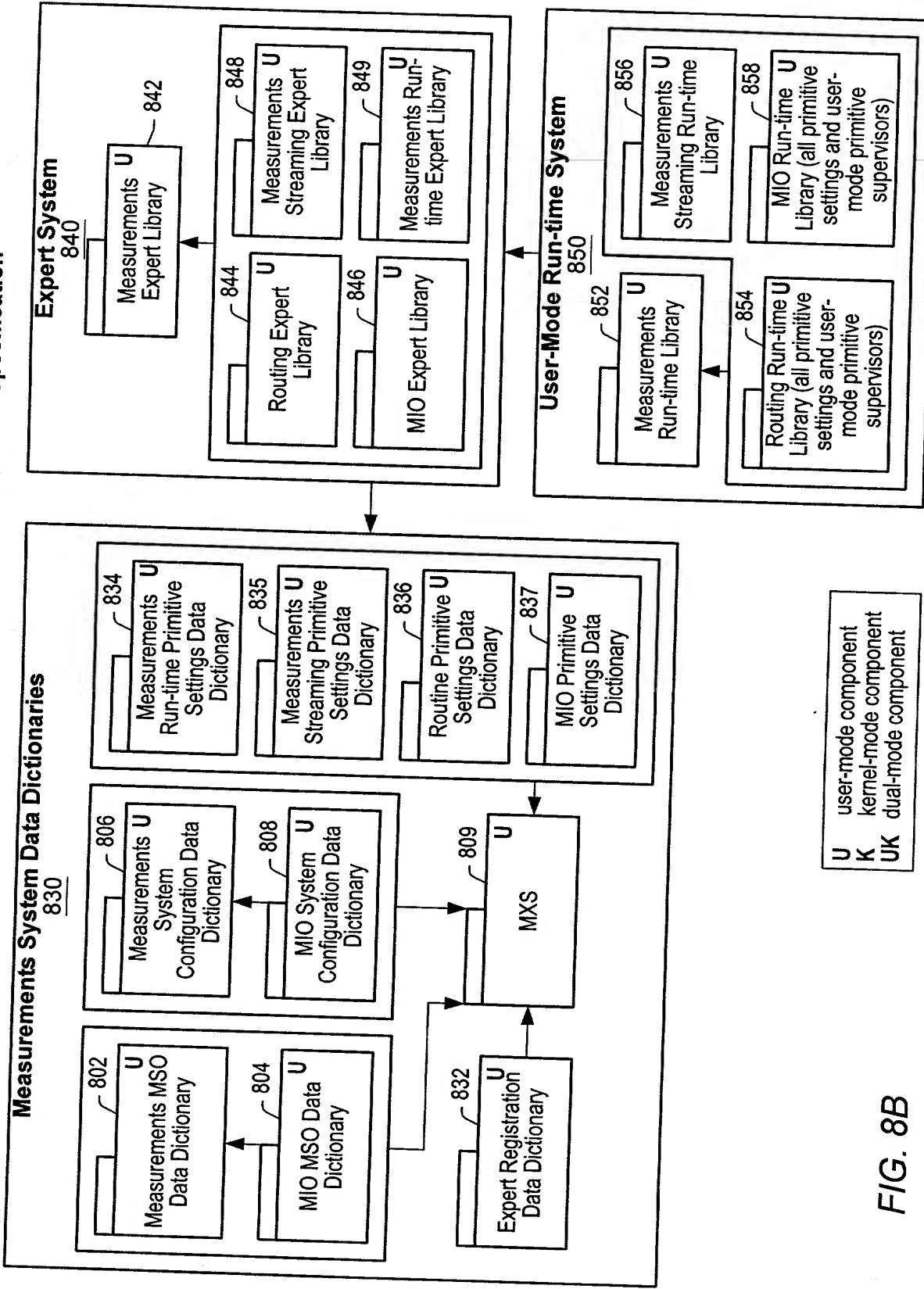


FIG. 8B

**Packages for Building Task Run-time from Run-time Specification**

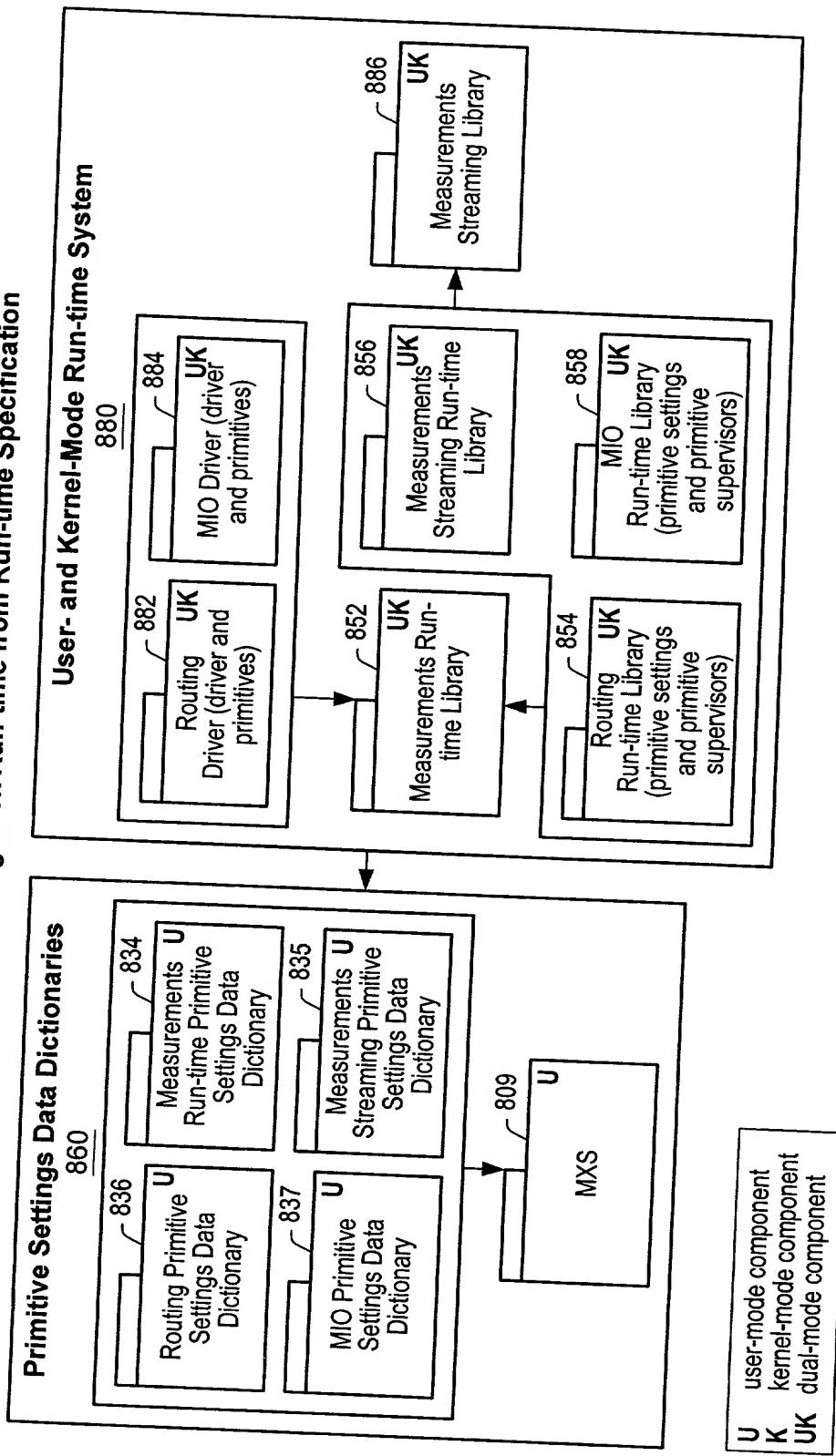


FIG. 8C

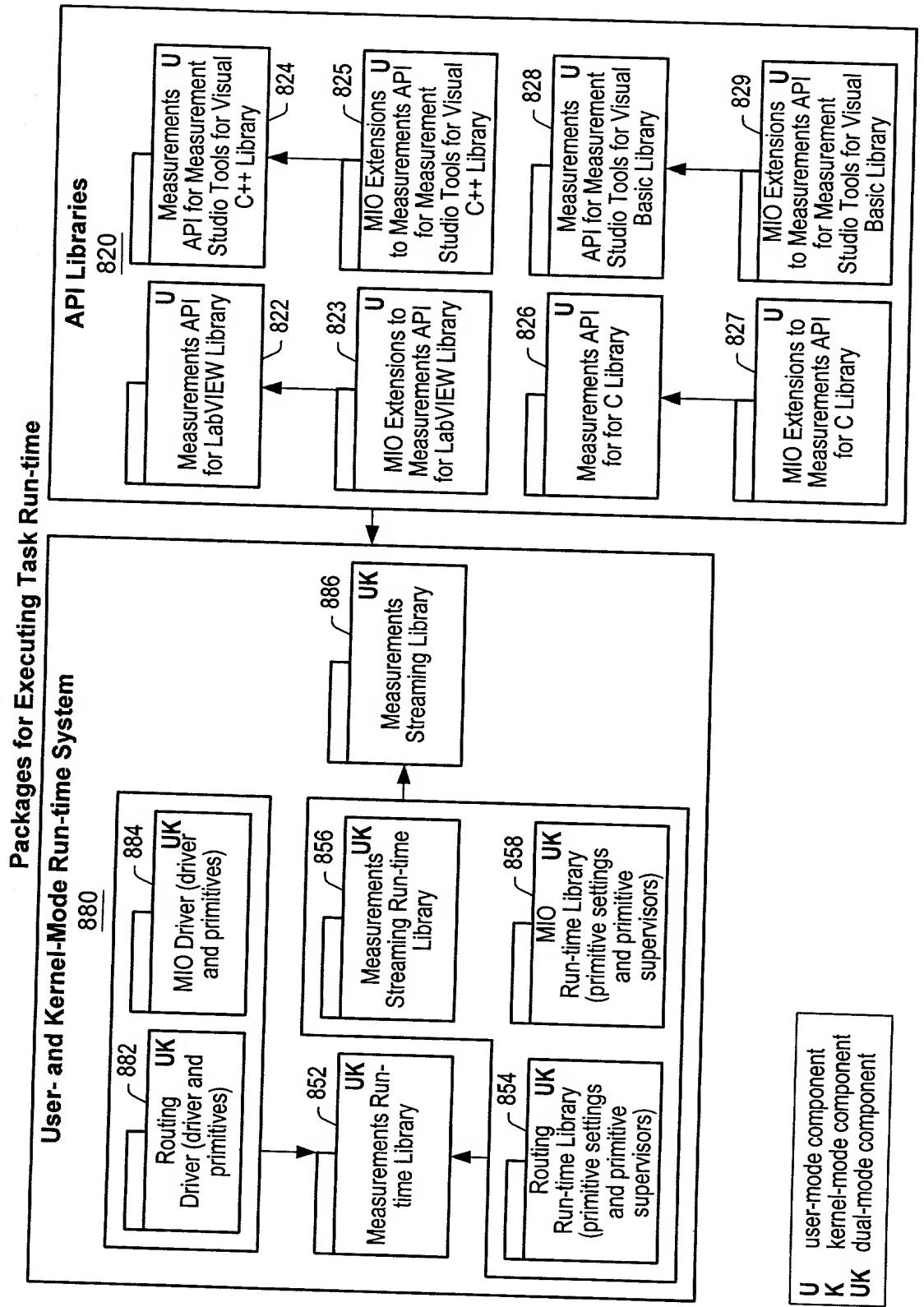
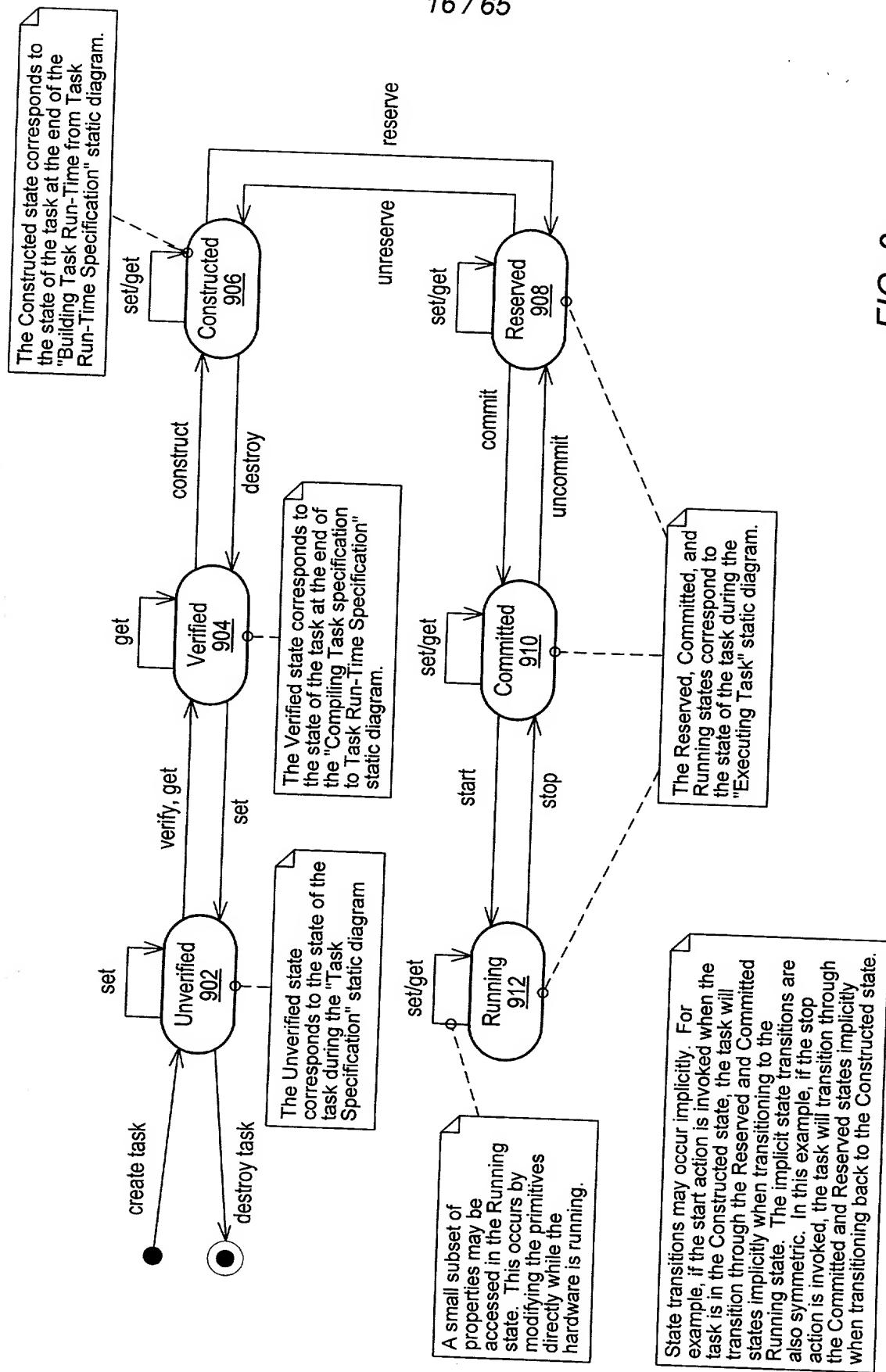


FIG. 8D

## State Diagram for Measurement Tasks

create task      destroy task      get      set      verify, get      construct      destroy      start      stop      commit      uncommit      reserve      unreserve



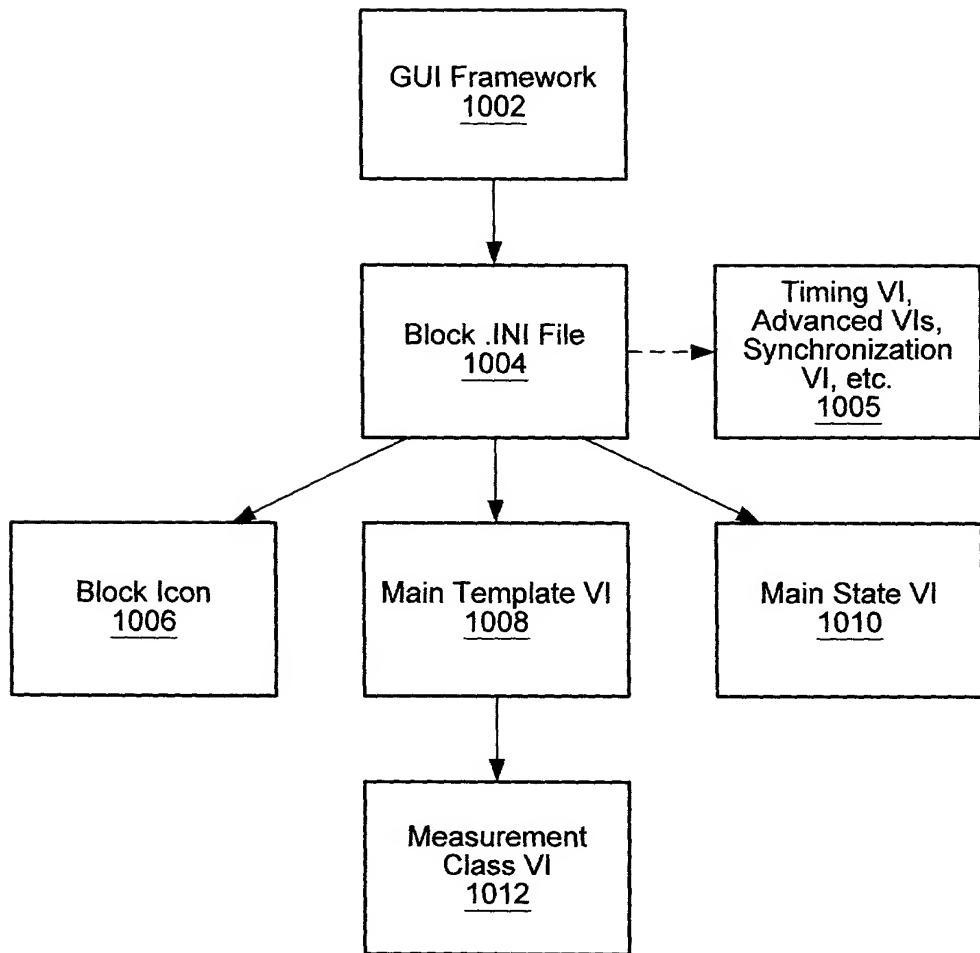


FIG. 10

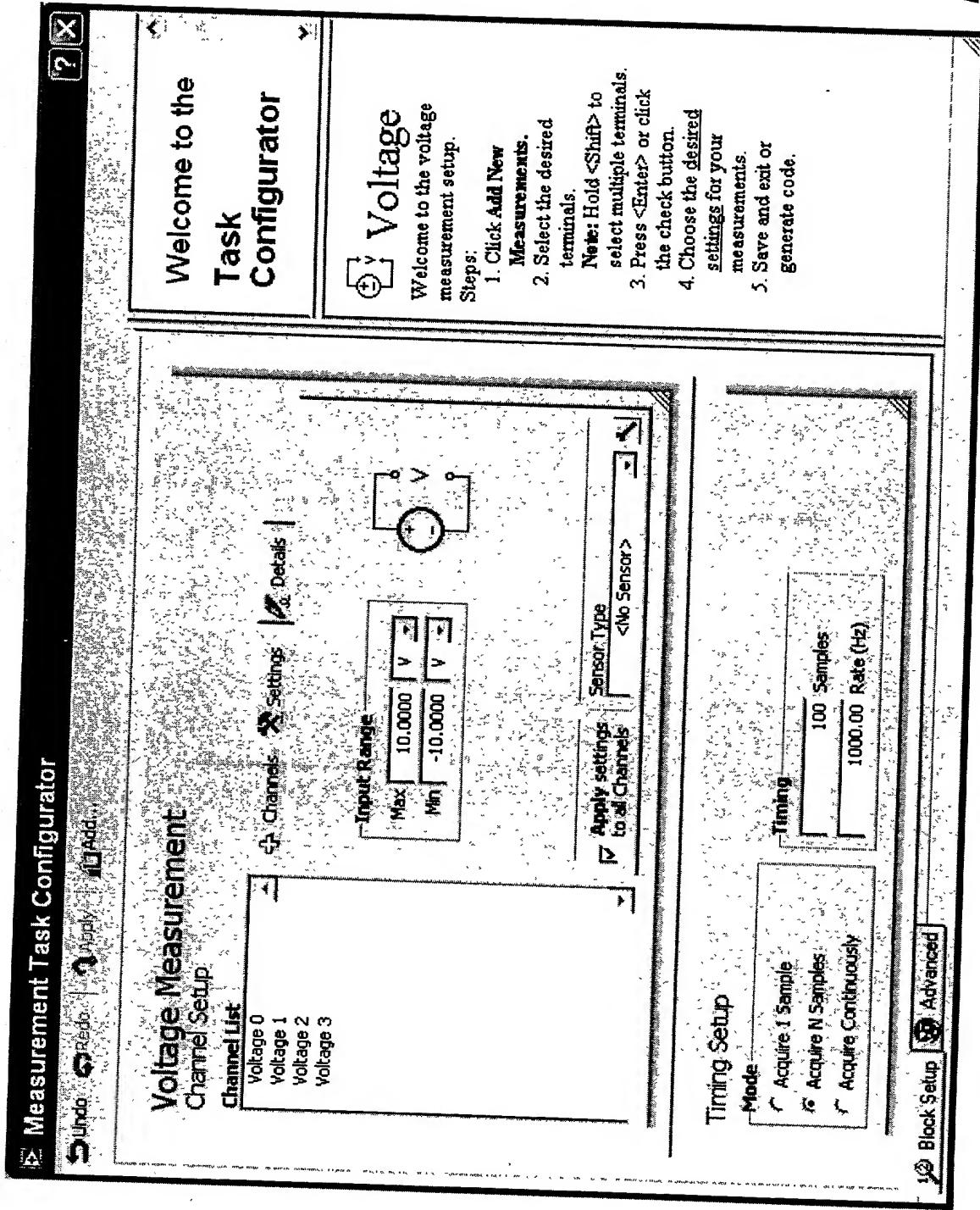


FIG. 11

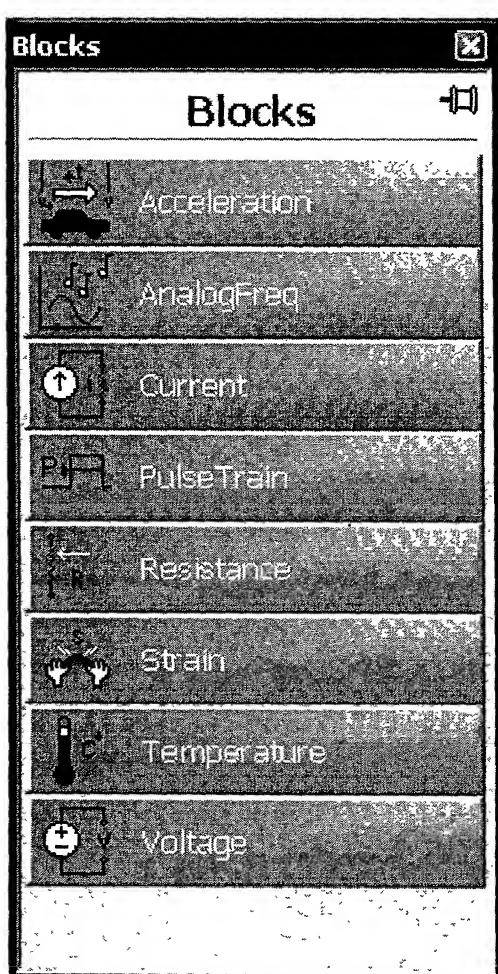
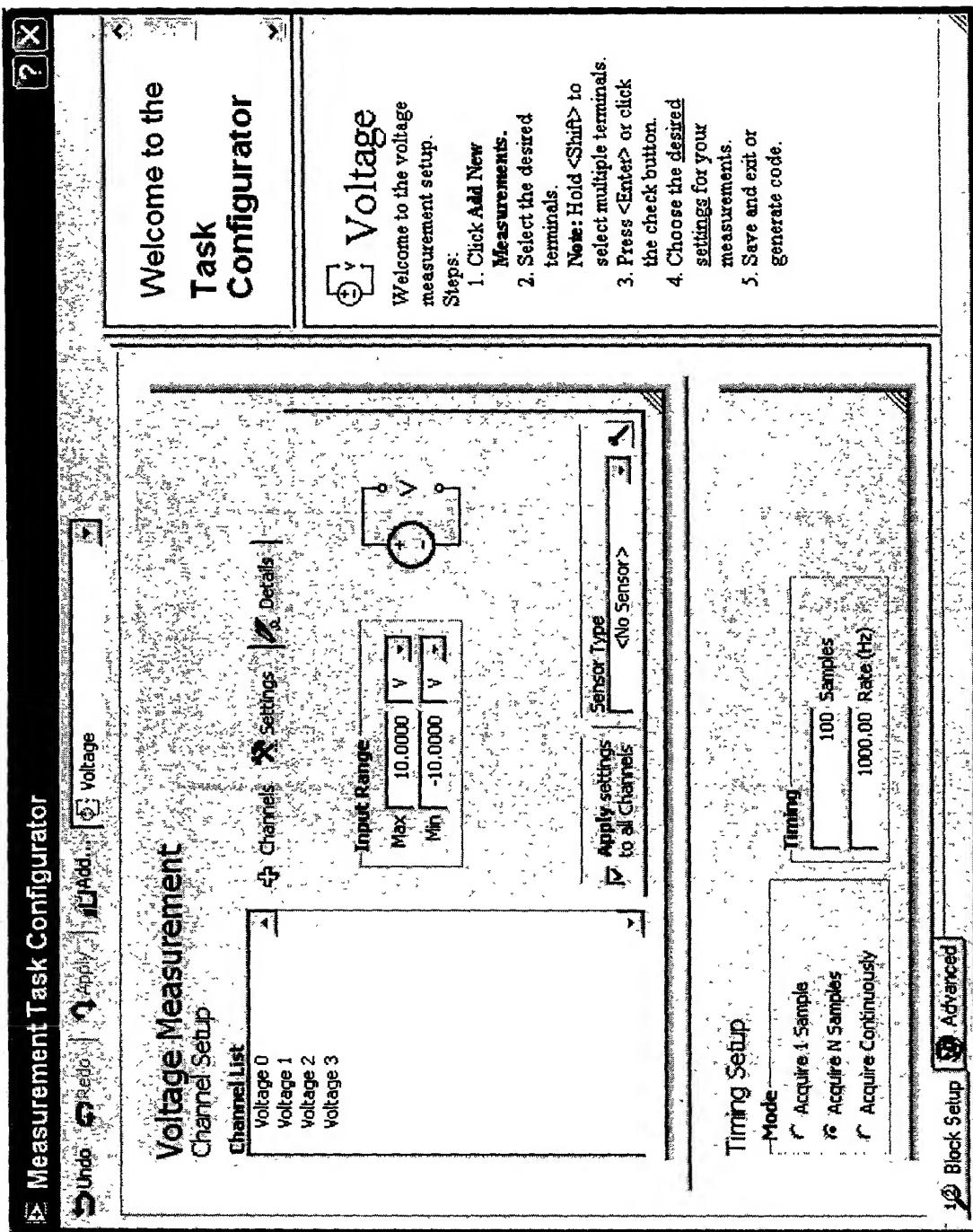


FIG. 12A

FIG. 12B



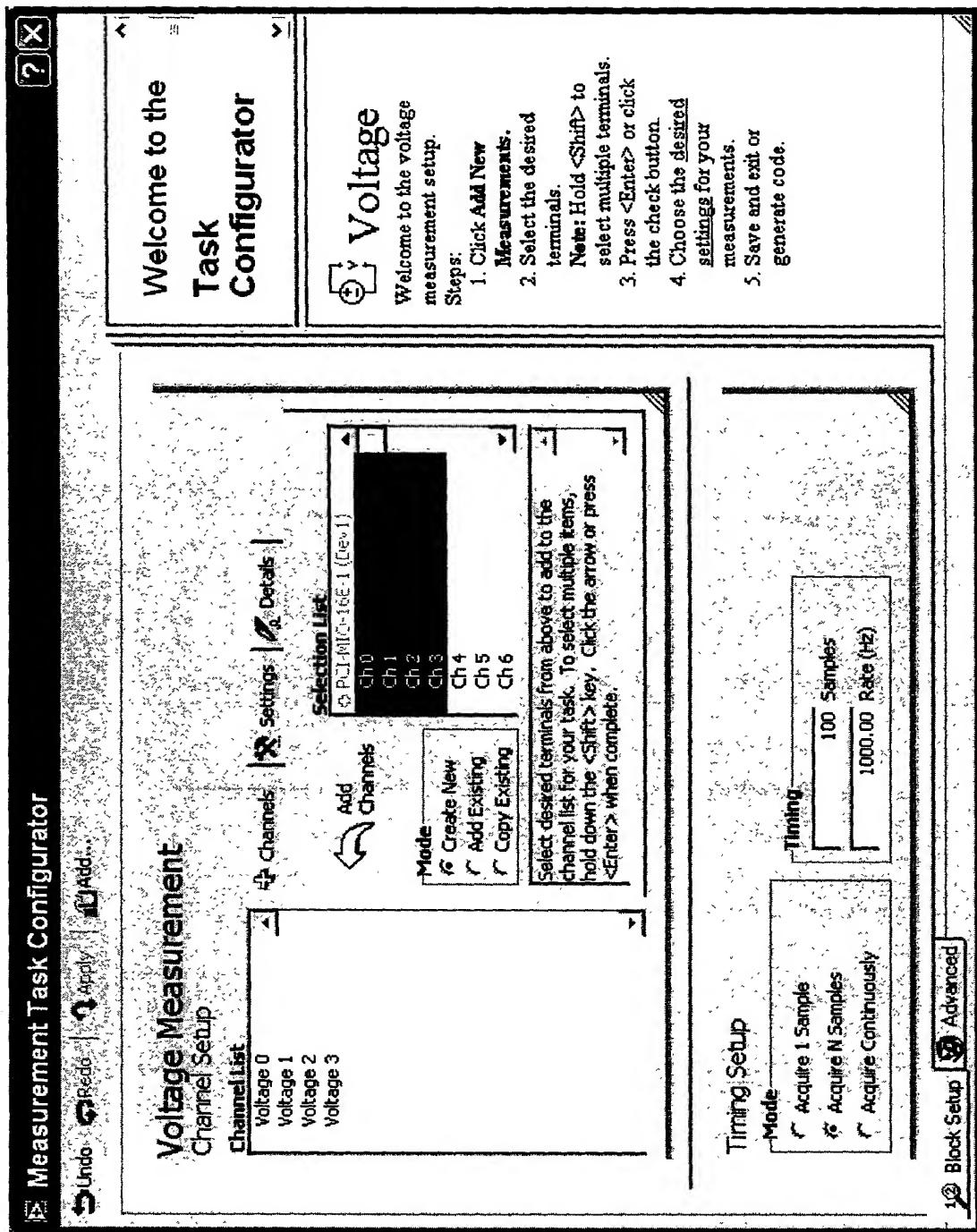


FIG. 12C

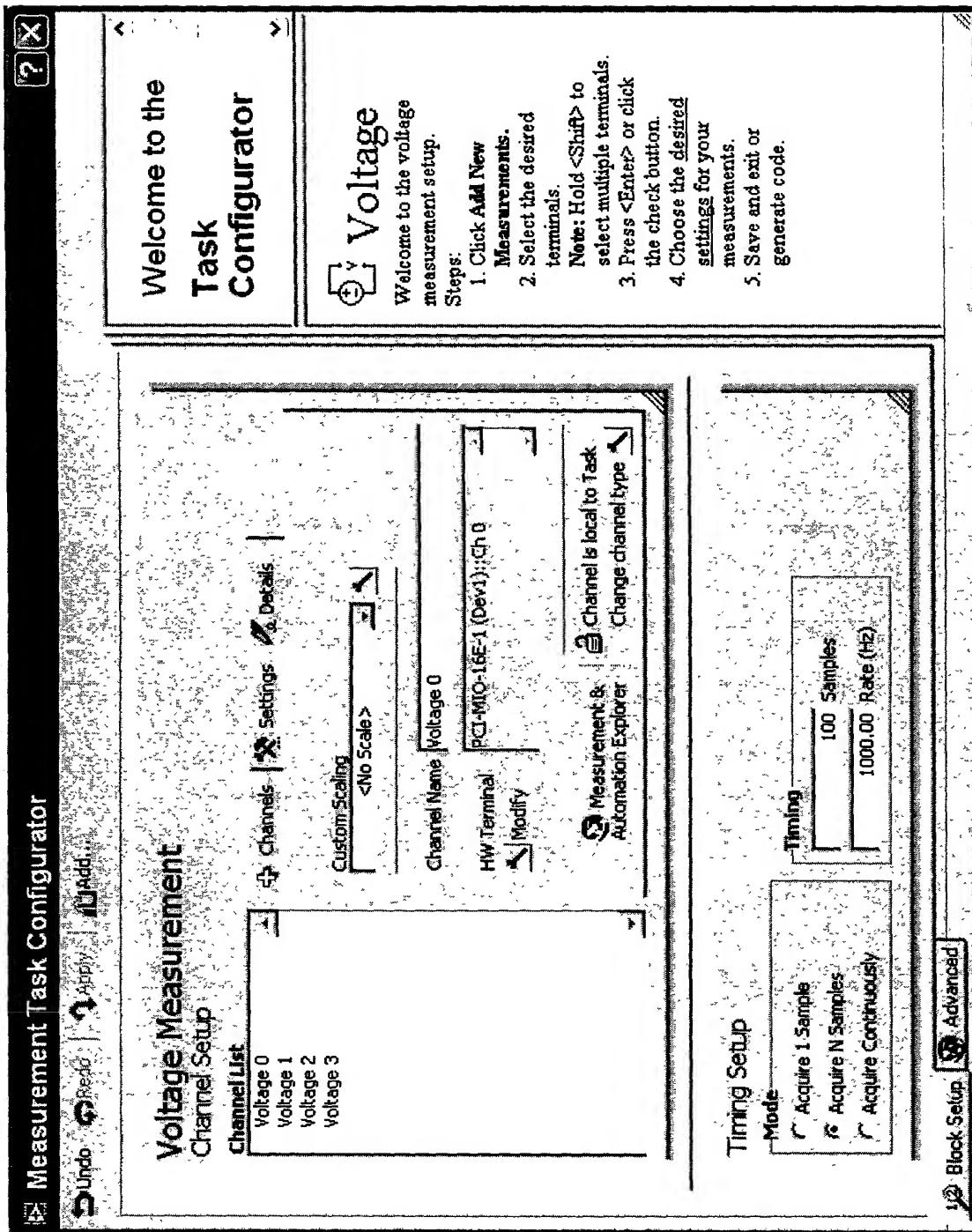


FIG. 12D

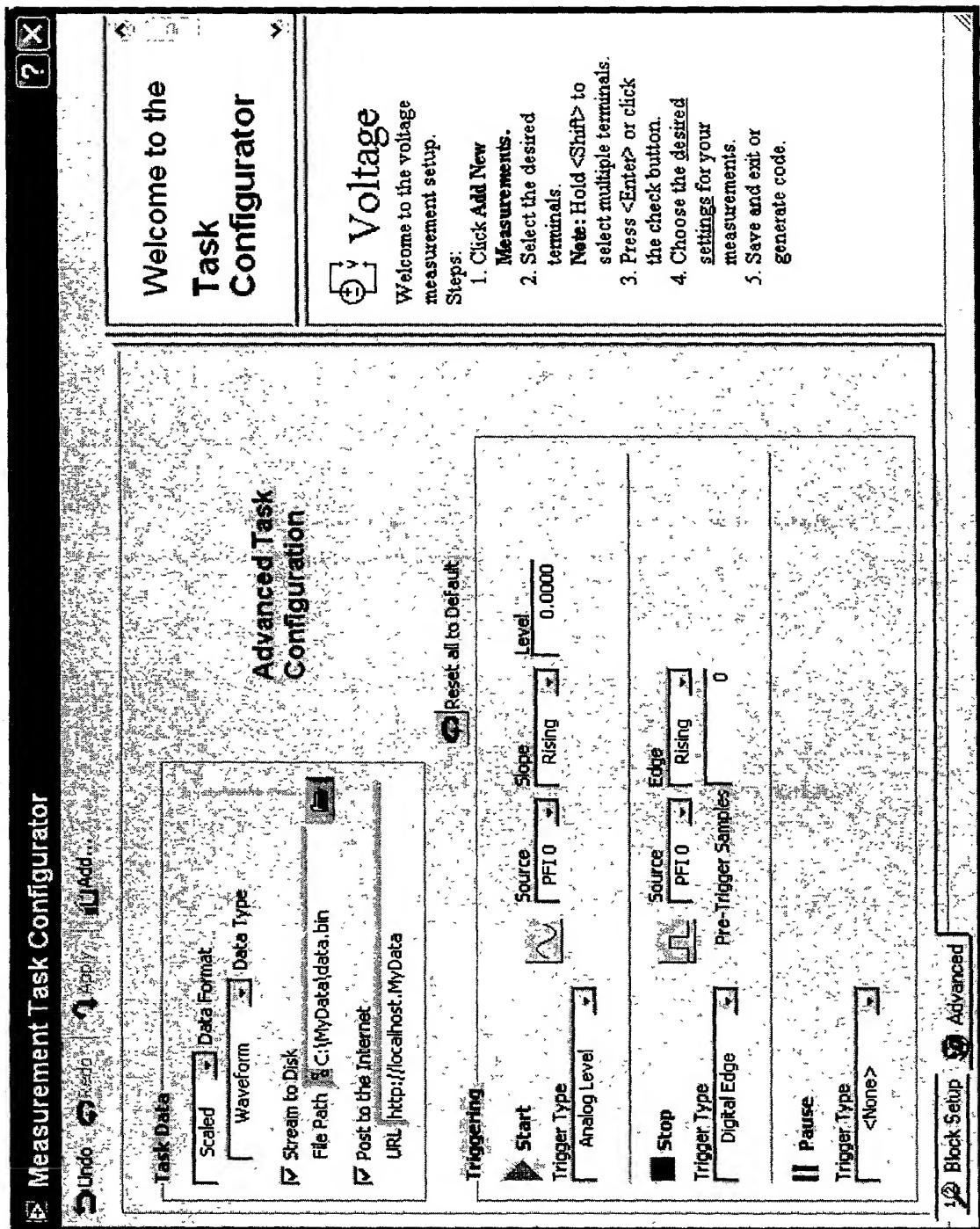
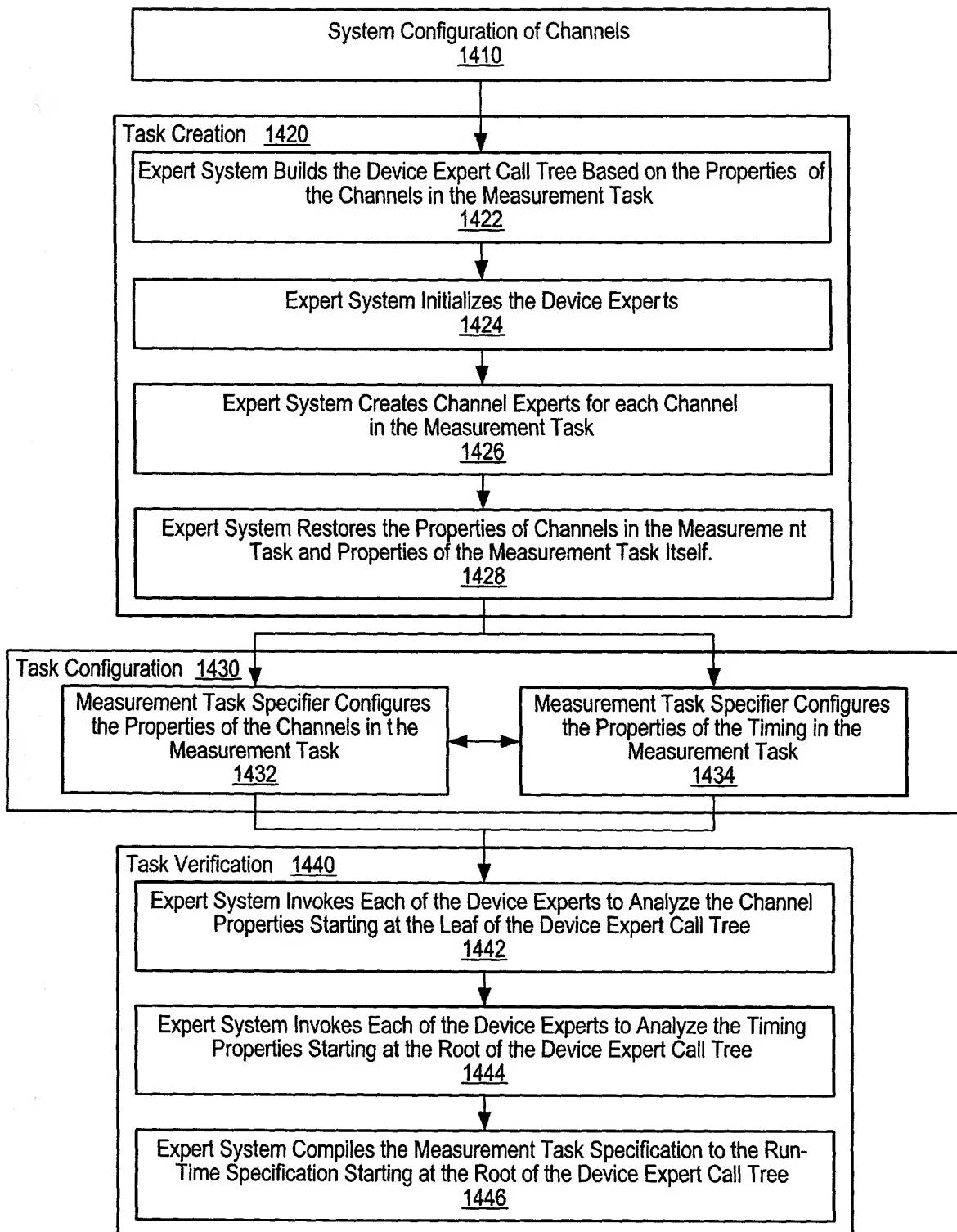


FIG. 13

**FIG. 14**

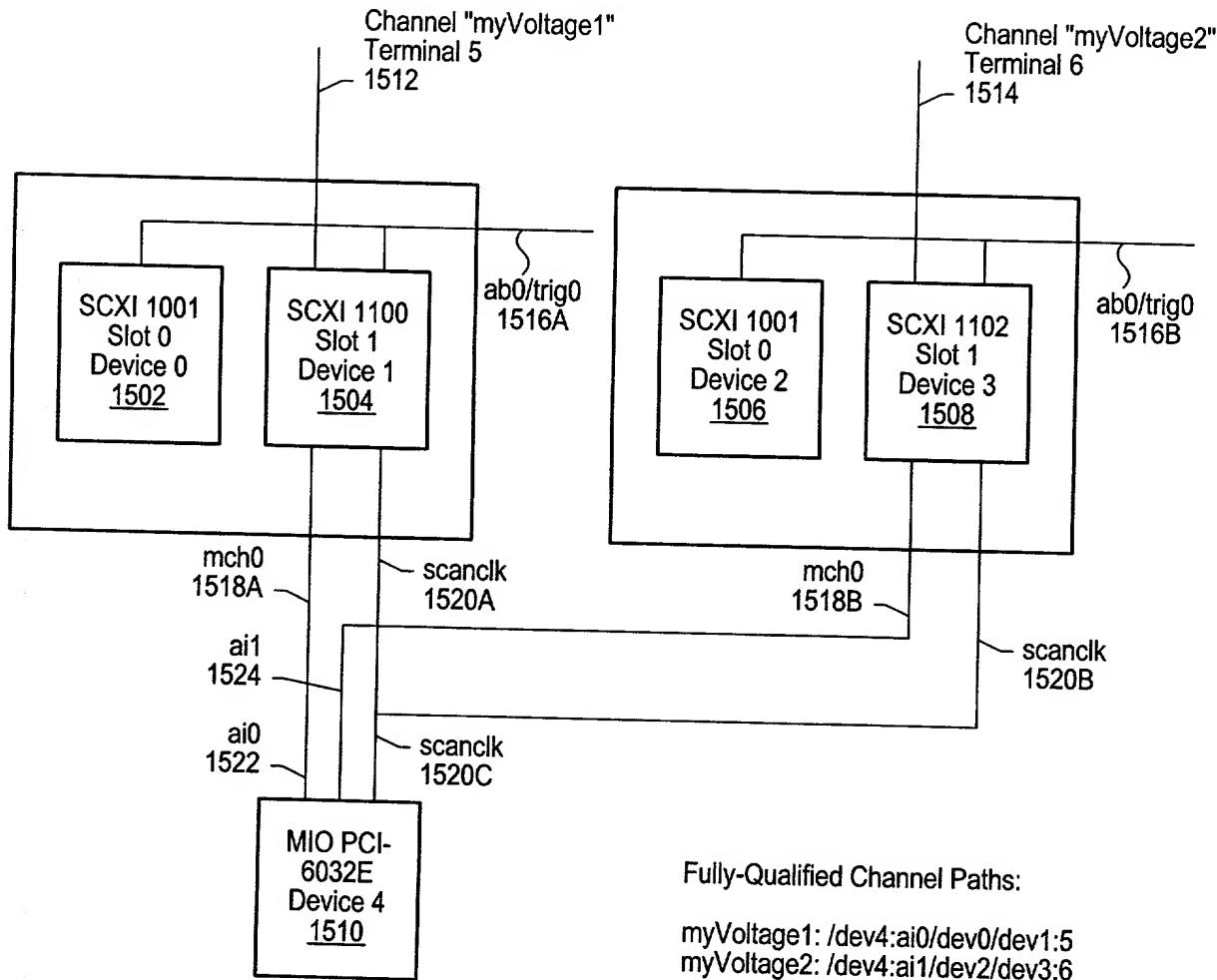
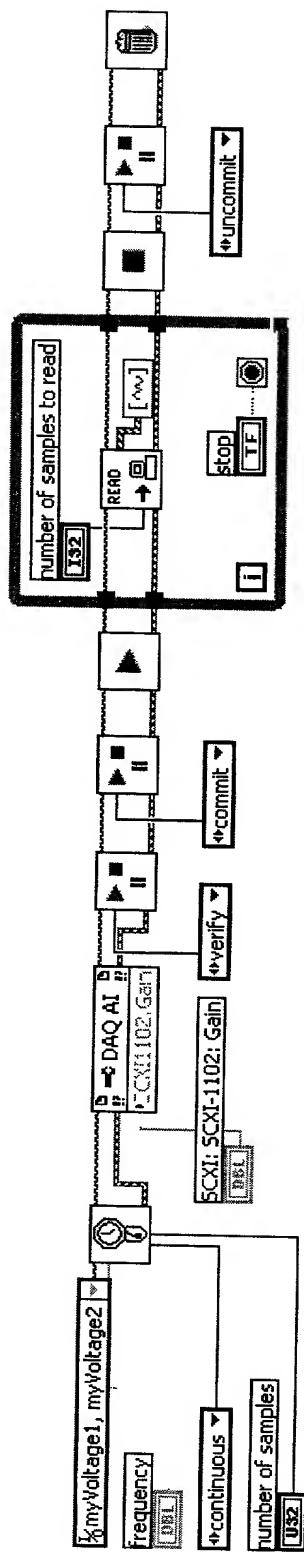


FIG. 15

10008792 • 022802



## Voltage On Two Channels with Two SCXI Modules in Two SCXI Chassis Connected to an MIO DAQ Device

FIG. 16

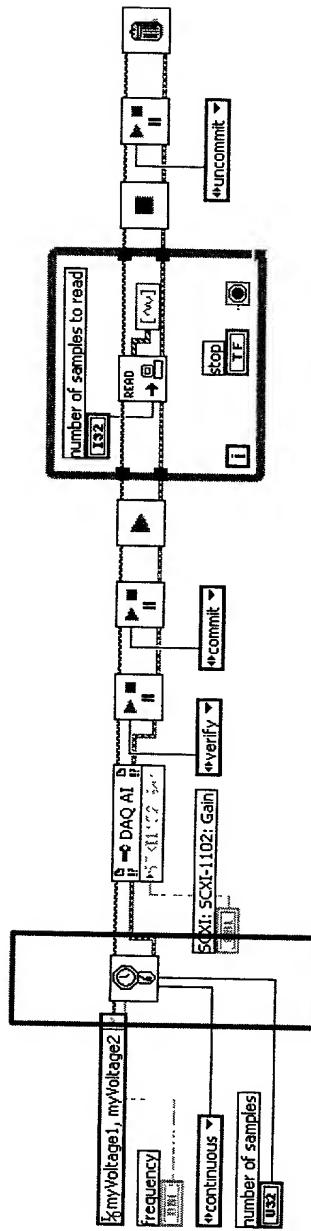
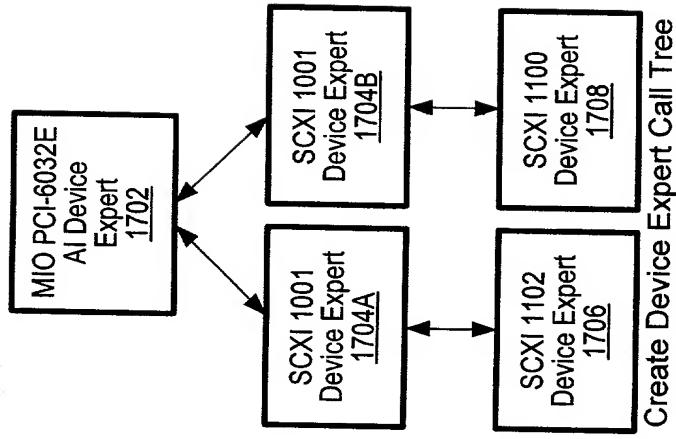


FIG. 17

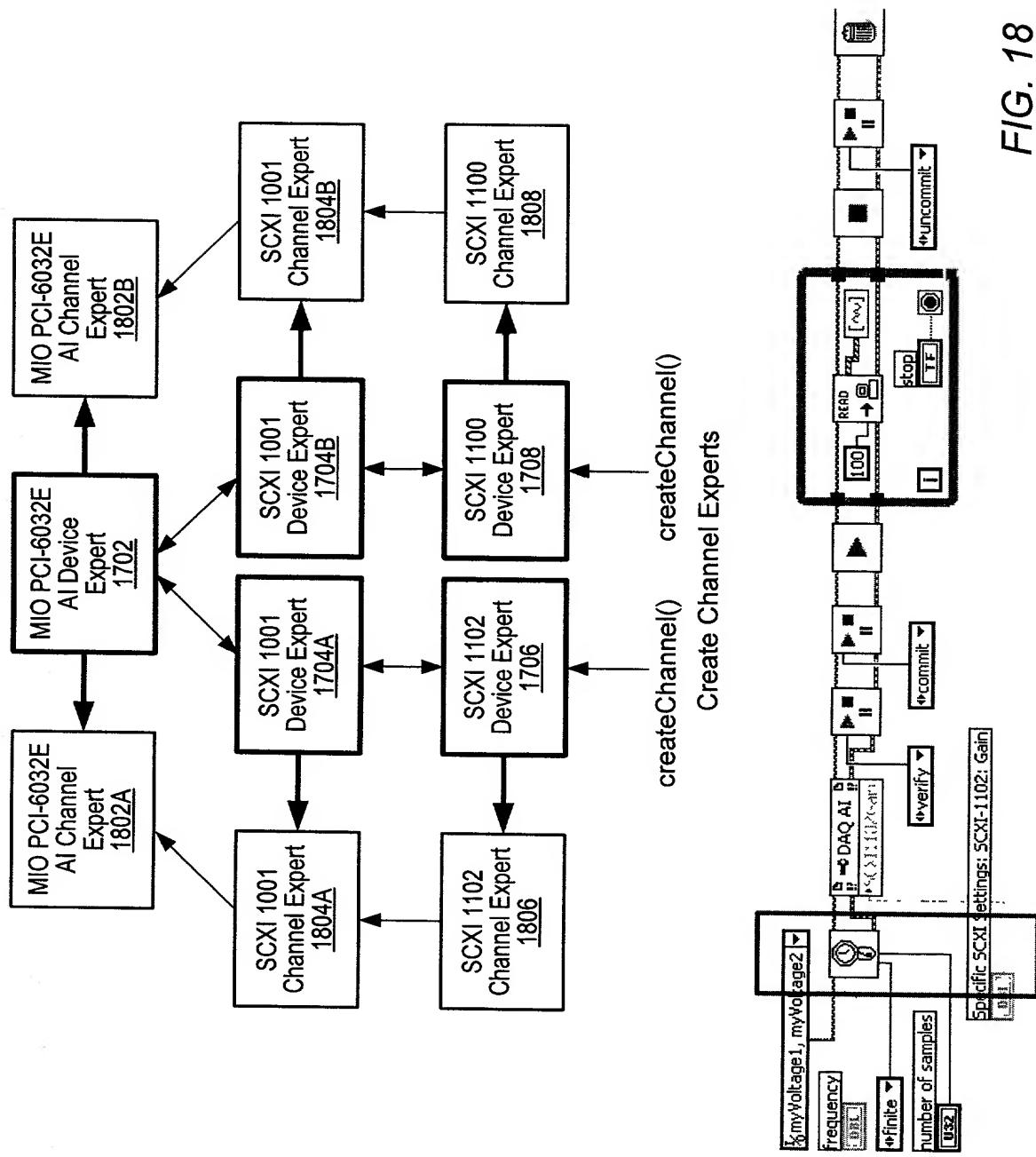
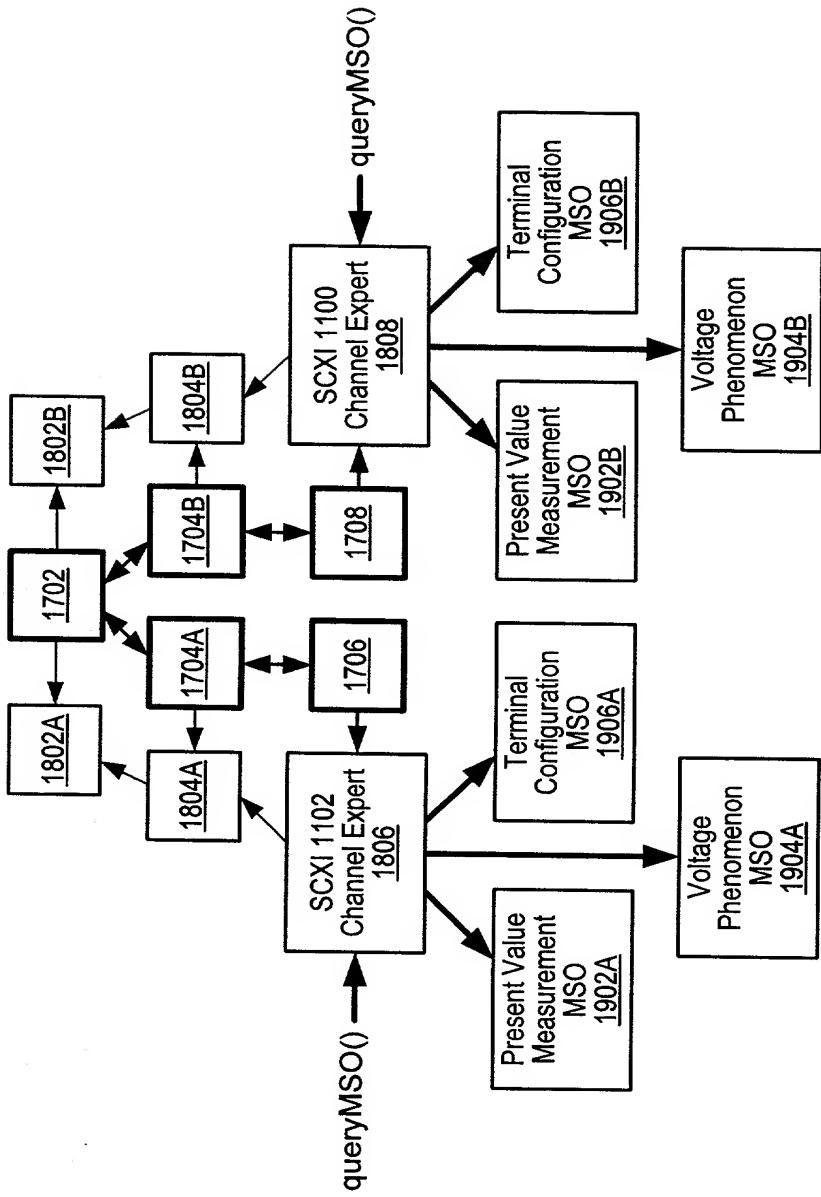
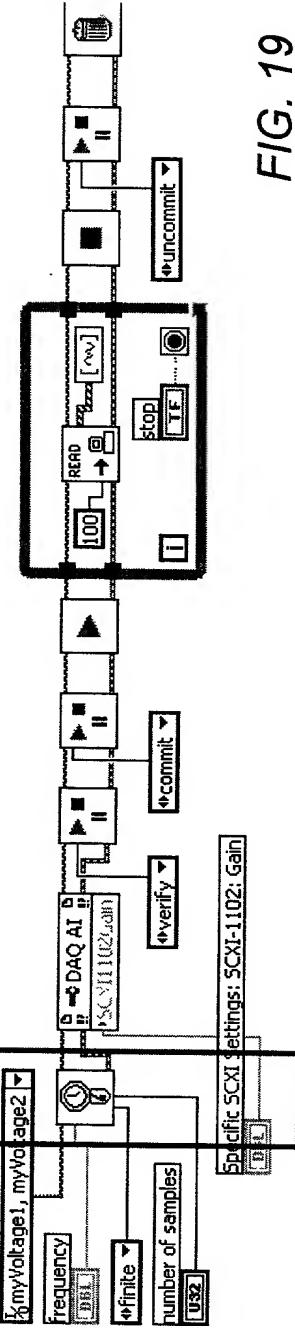


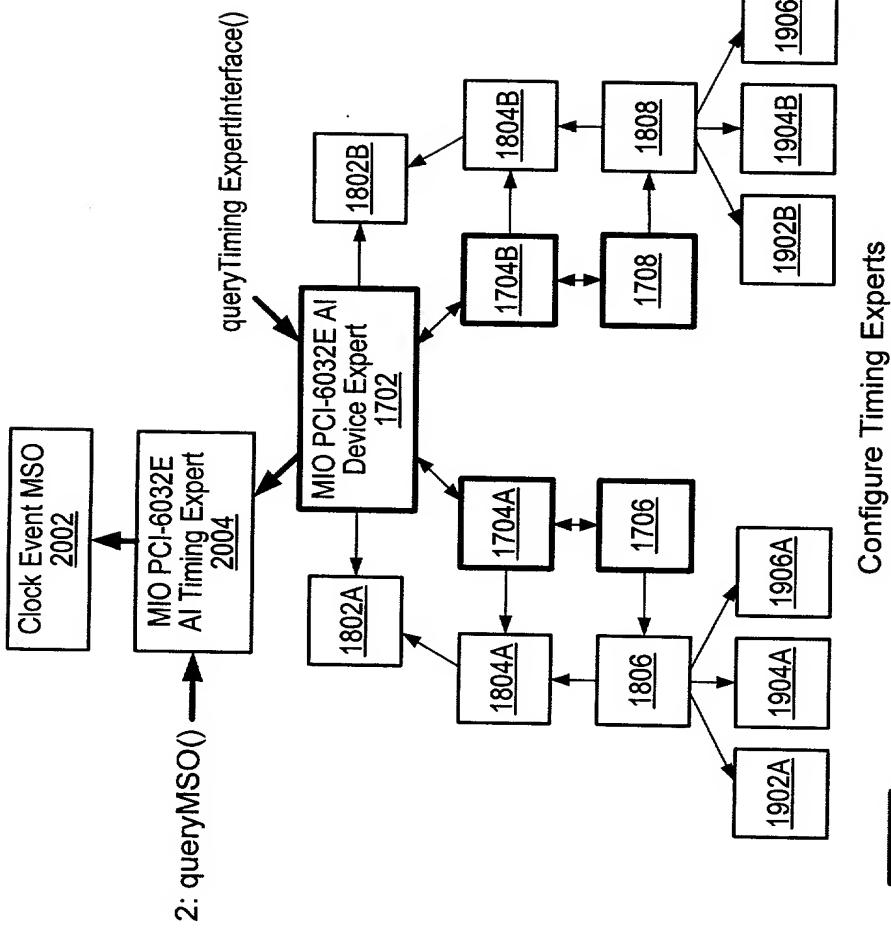
FIG. 18



Deserialize Named Channel MSOs



F/G. 19



Configure Timing Experts

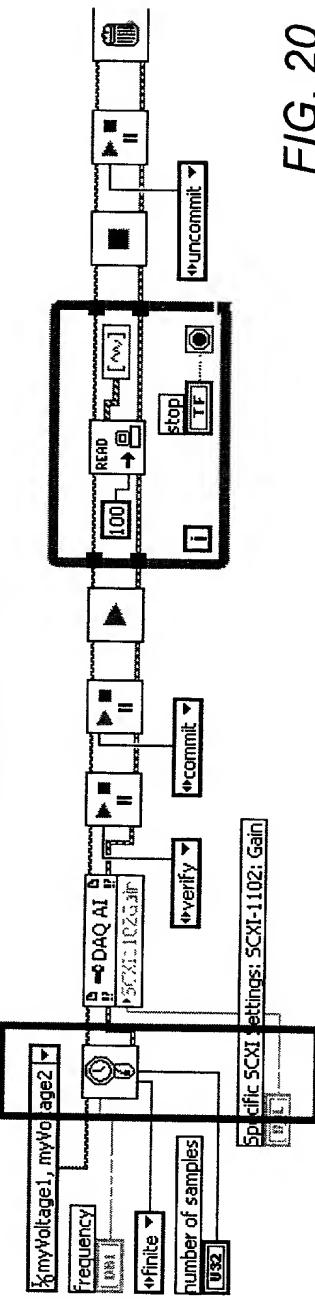


FIG. 20

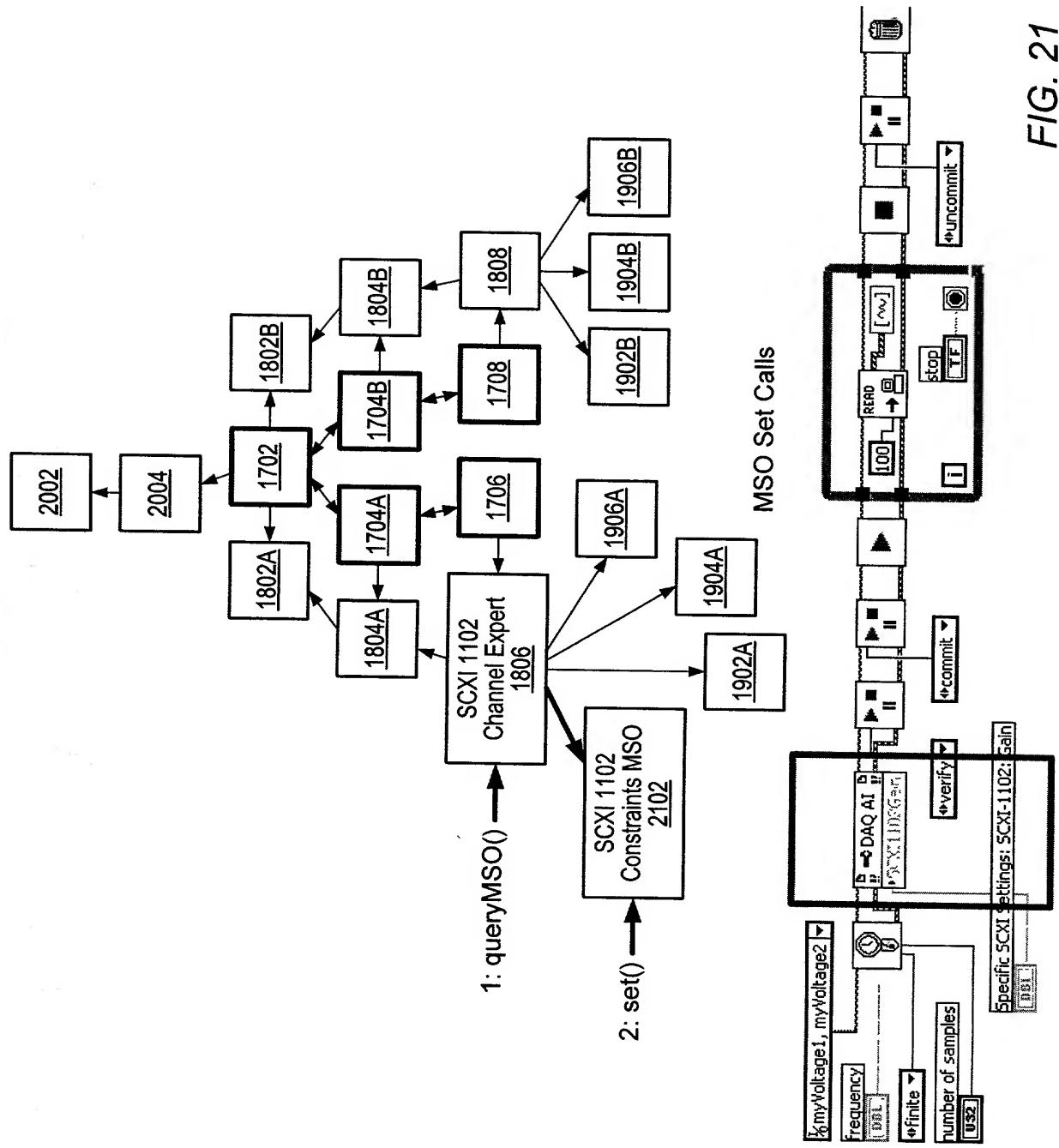


FIG. 21

4000002.032000E

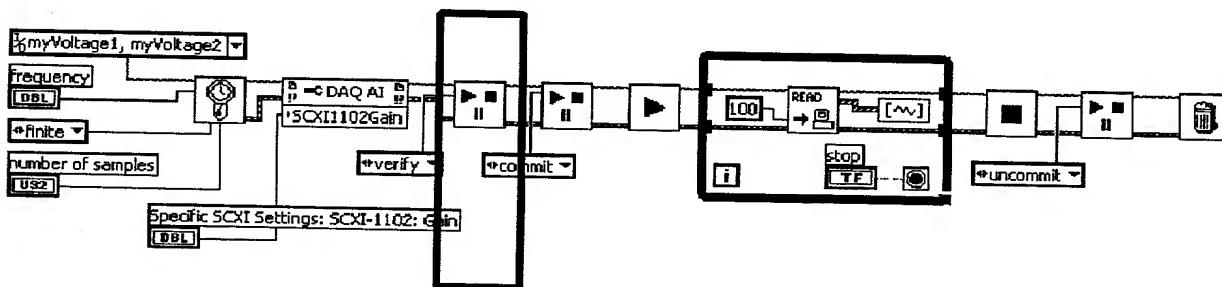
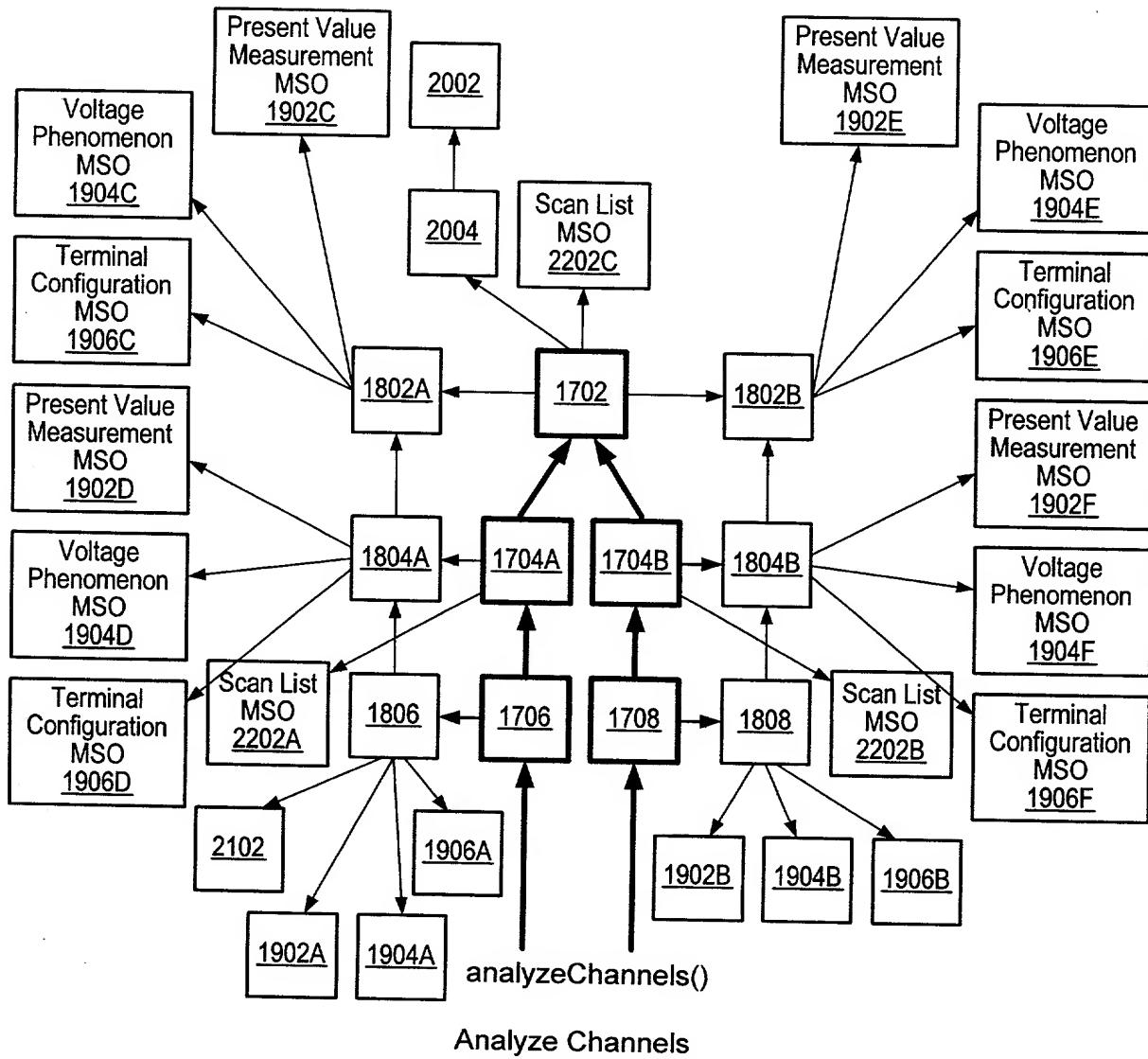


FIG. 22

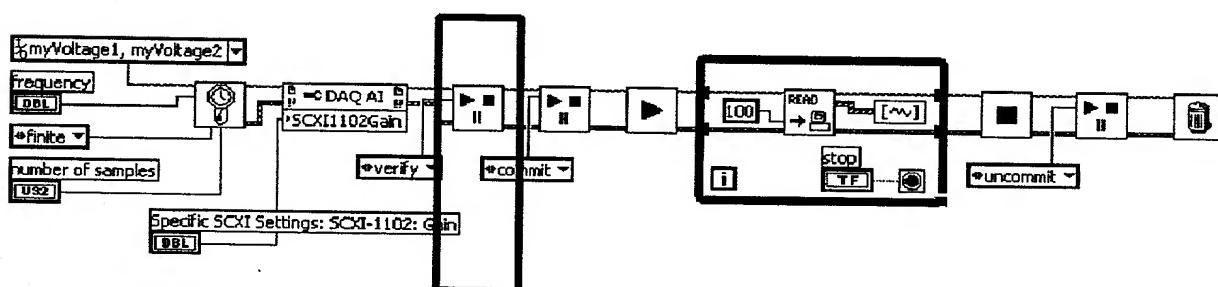
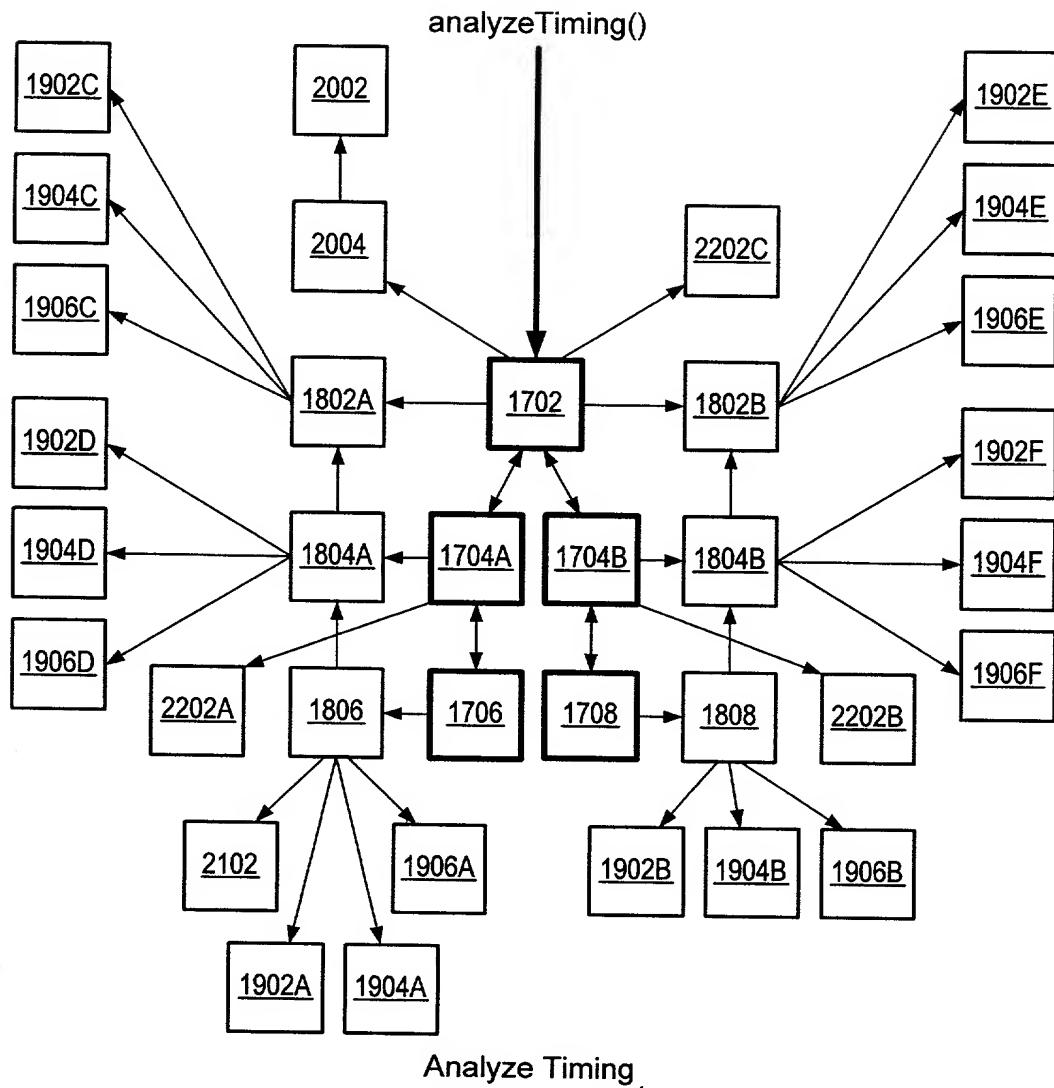


FIG. 23

1.00087928.CORES.DOC

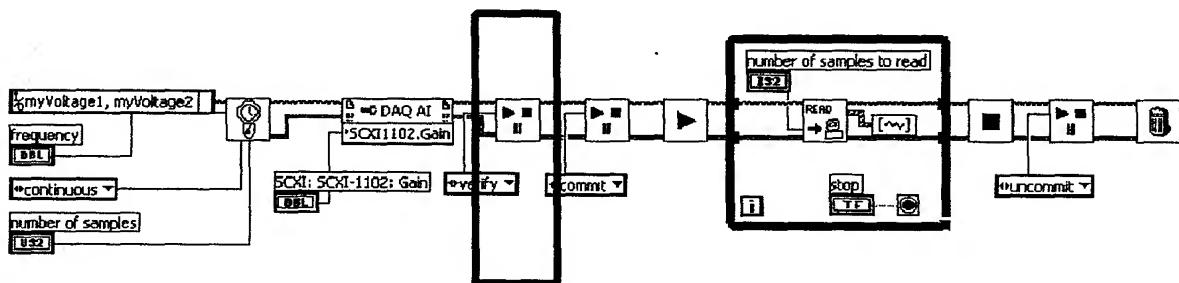
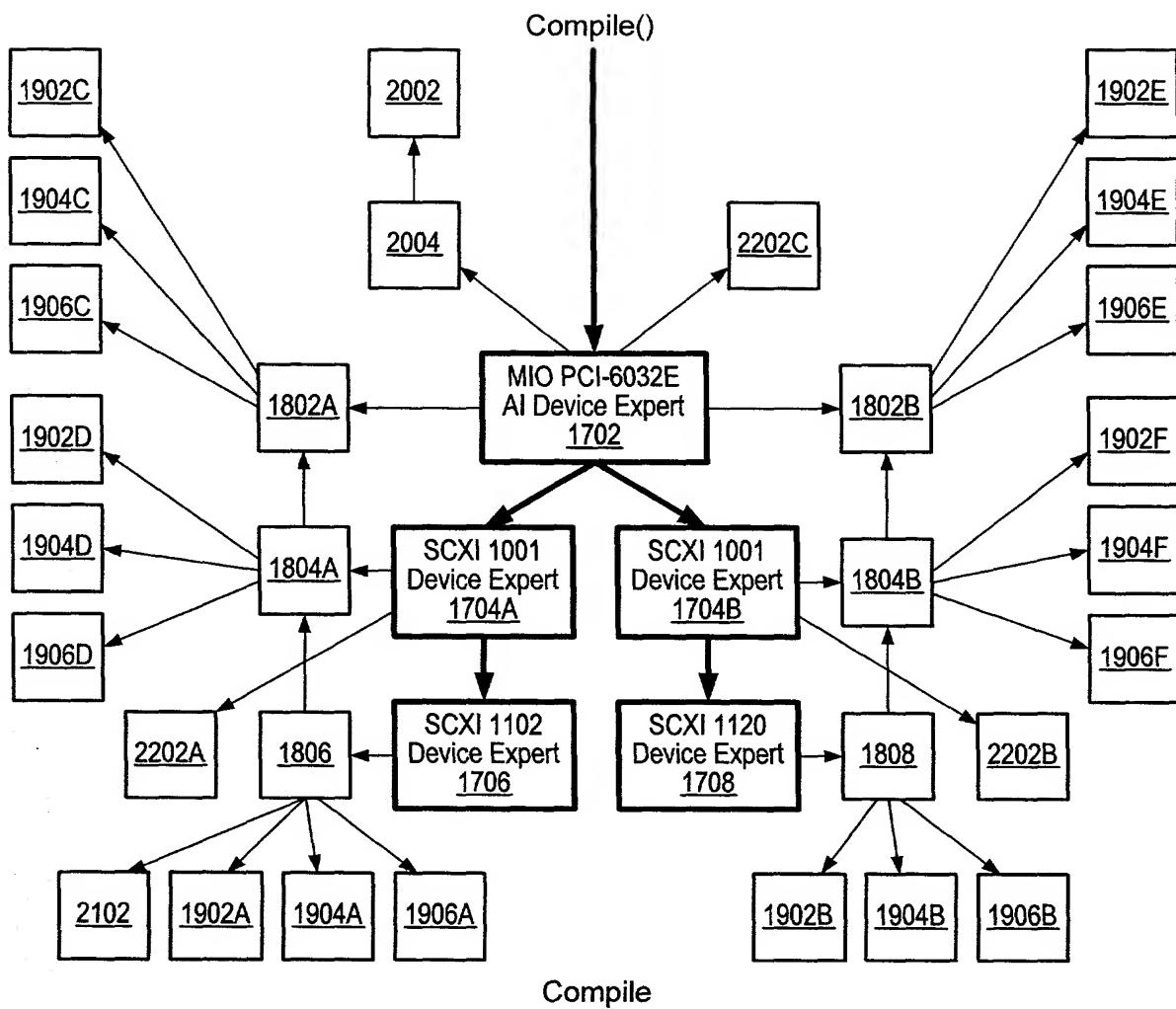


FIG. 24A

10008792 - 083003

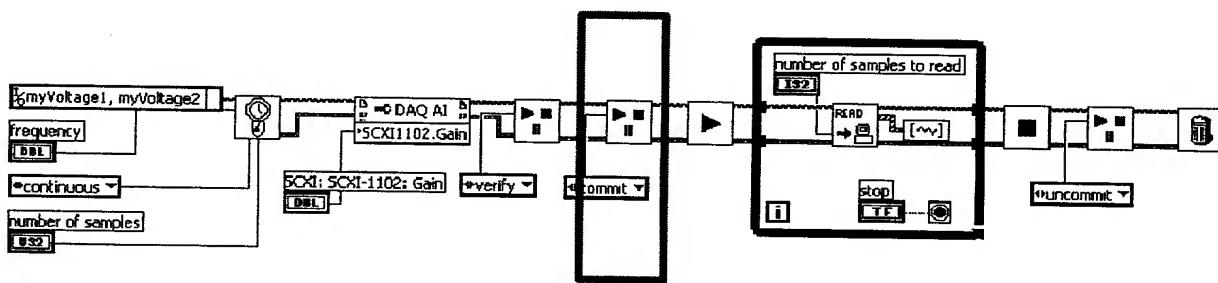
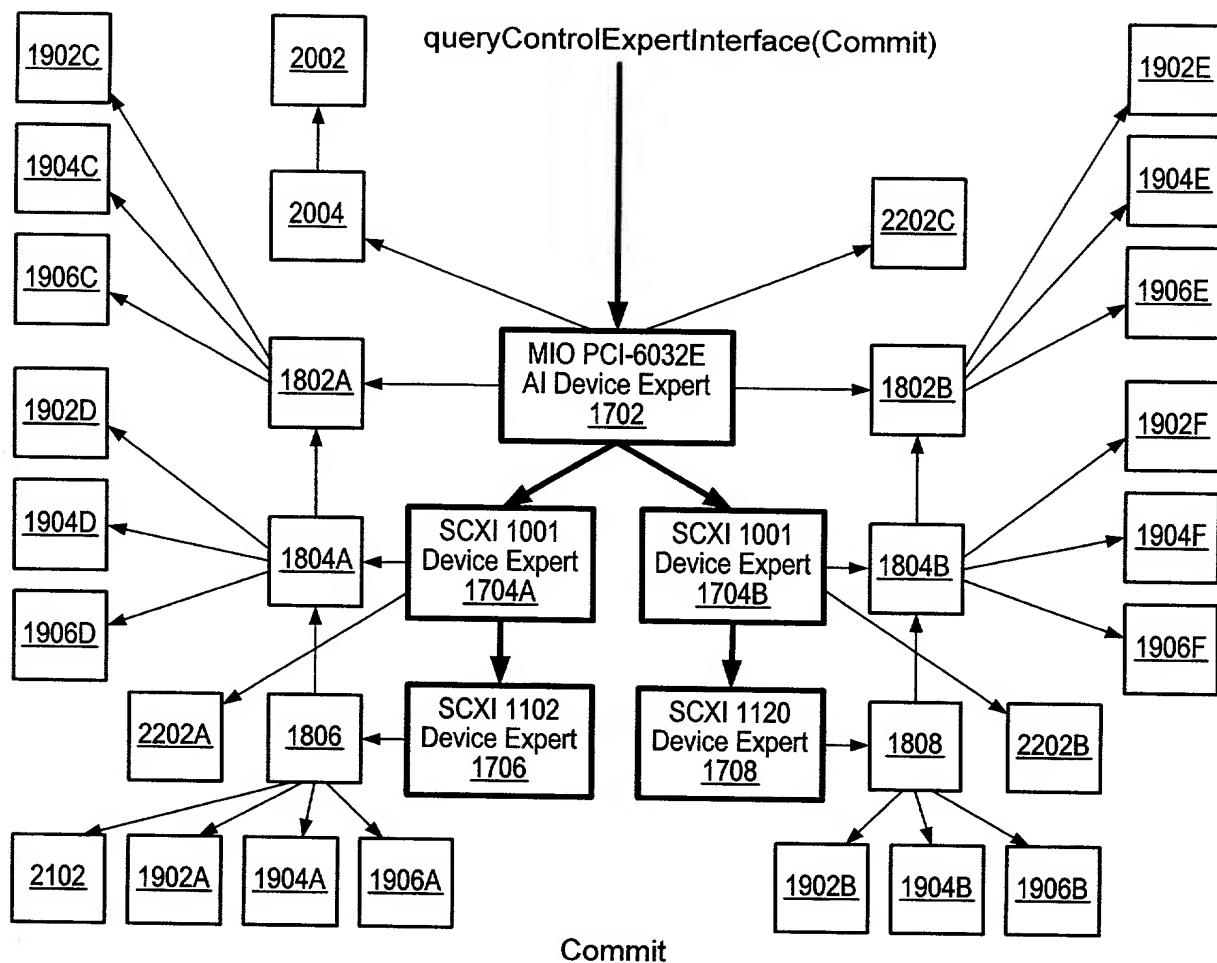


FIG. 24B

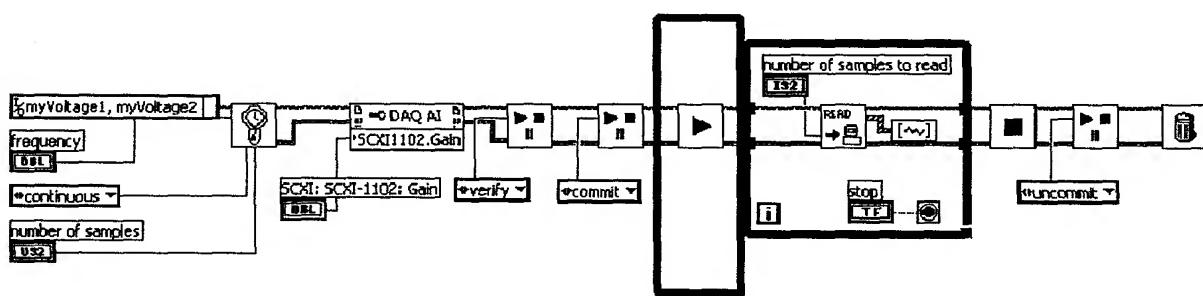
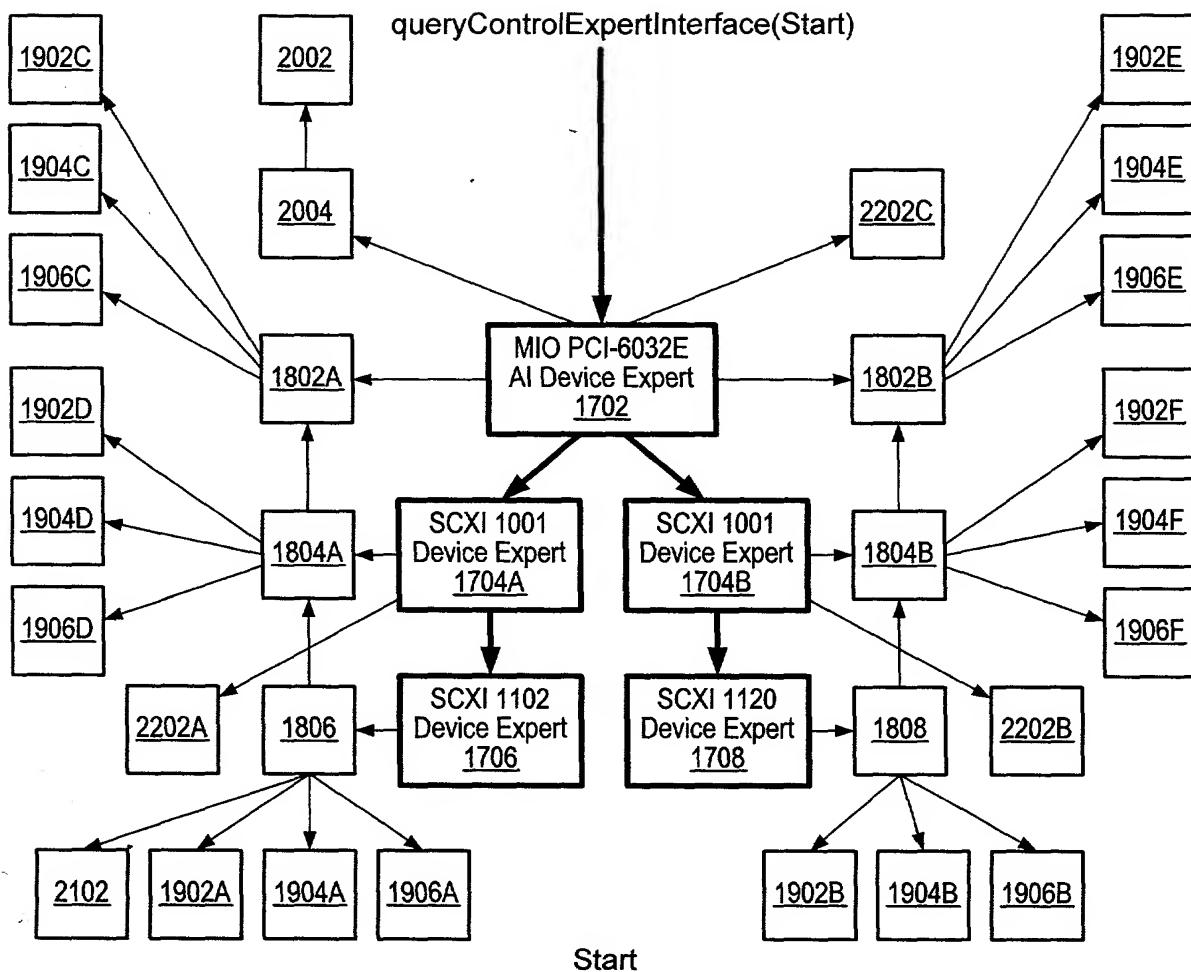


FIG. 24C

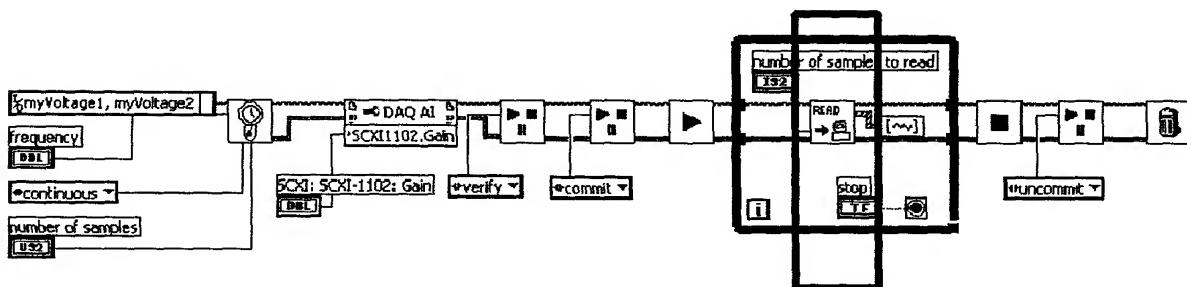
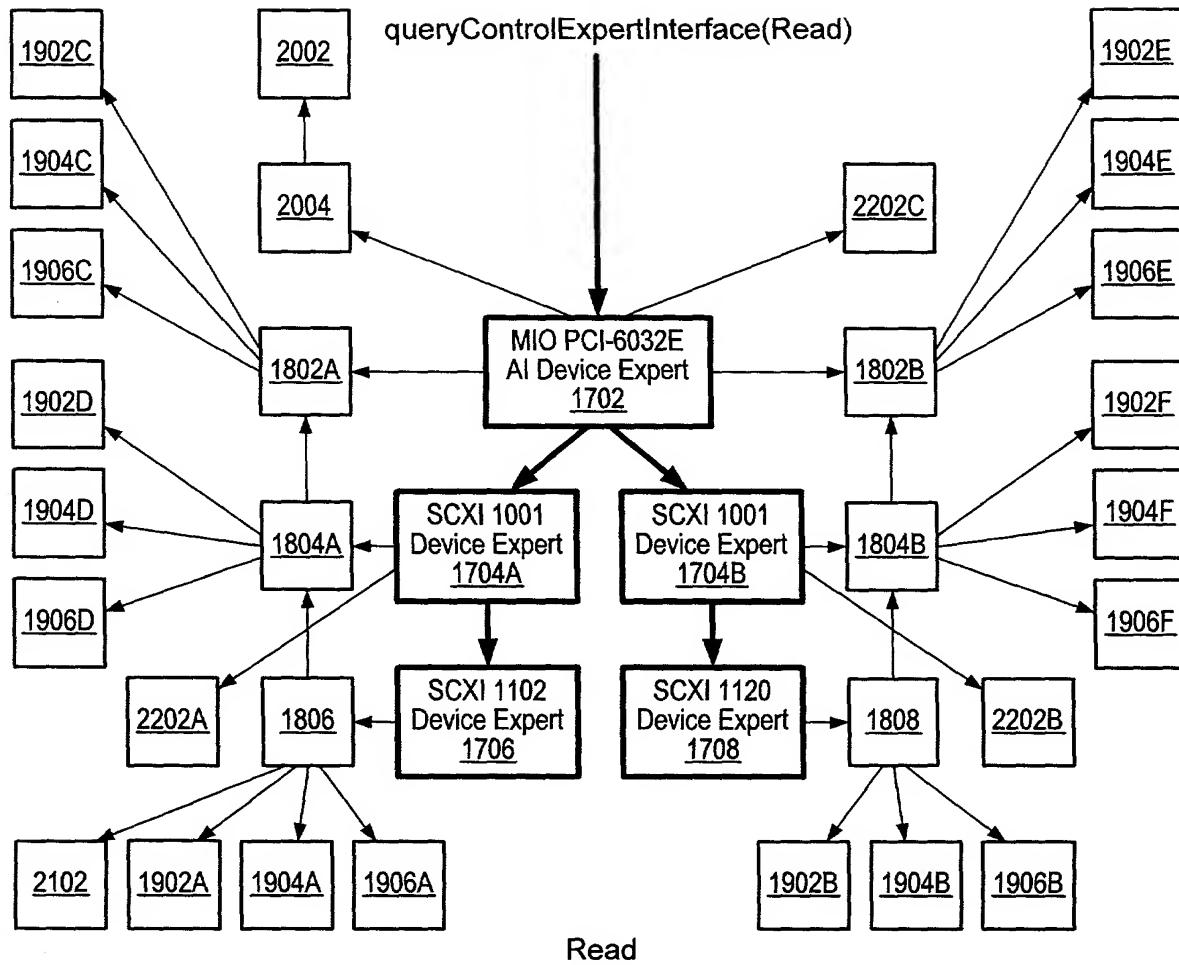


FIG. 24D

1.0000000000000000E+000

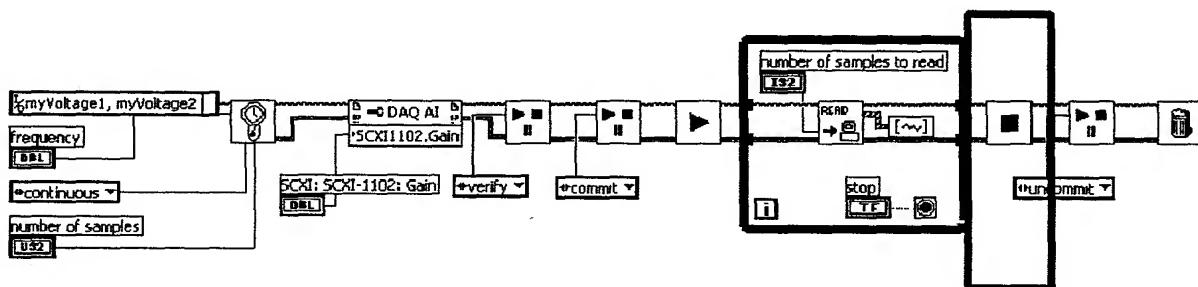
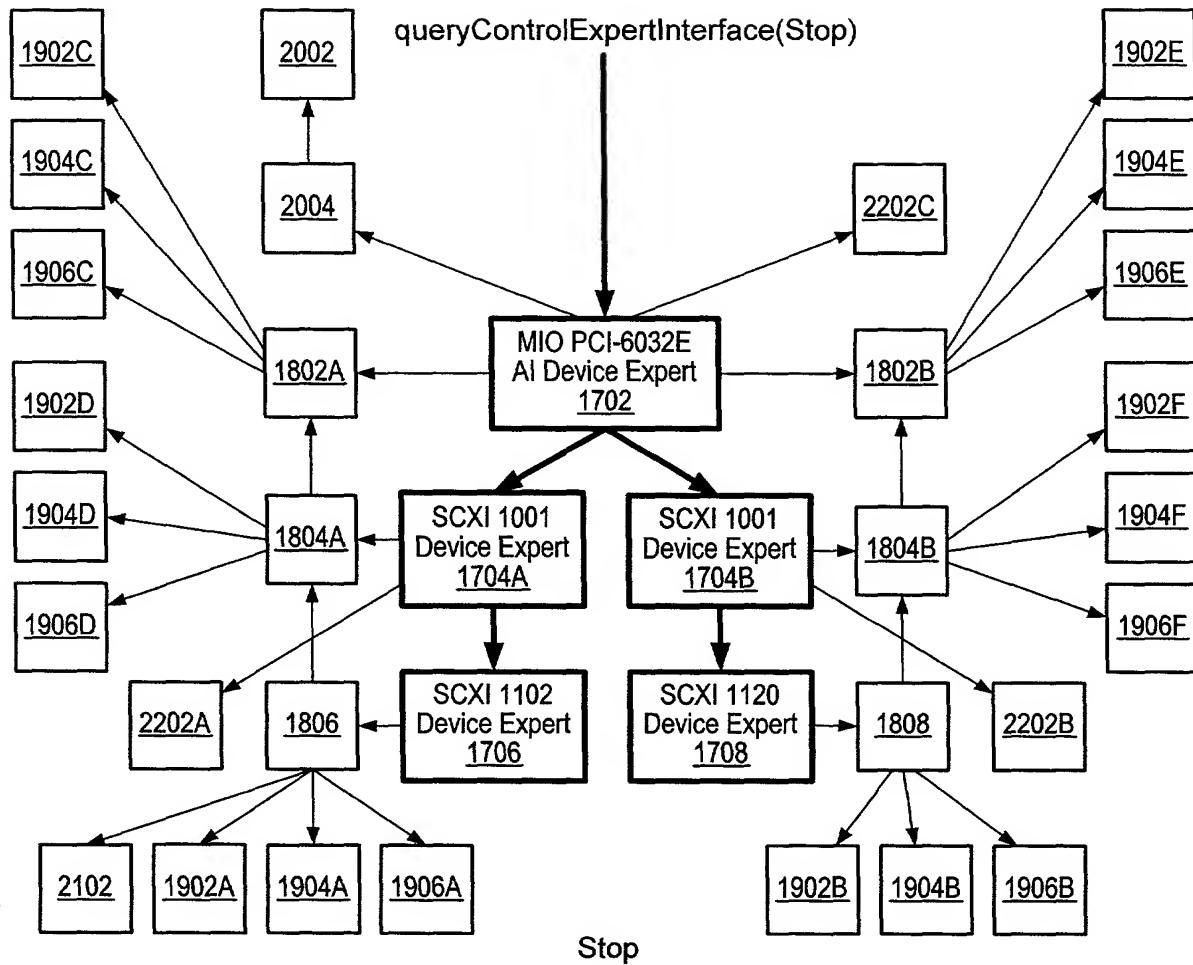


FIG. 24E

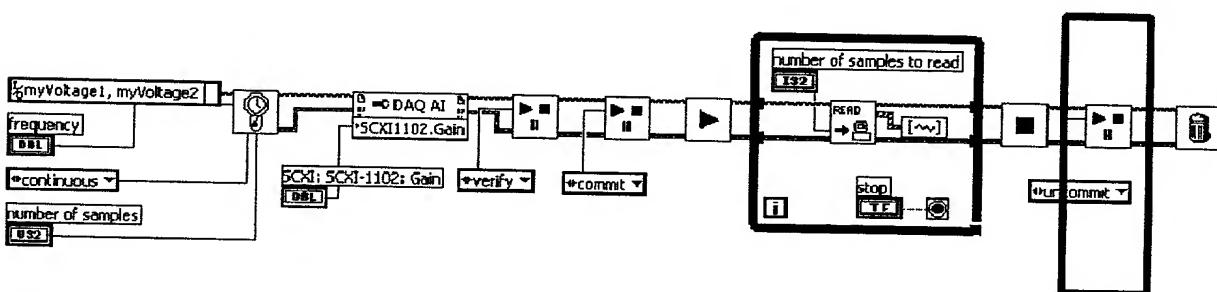
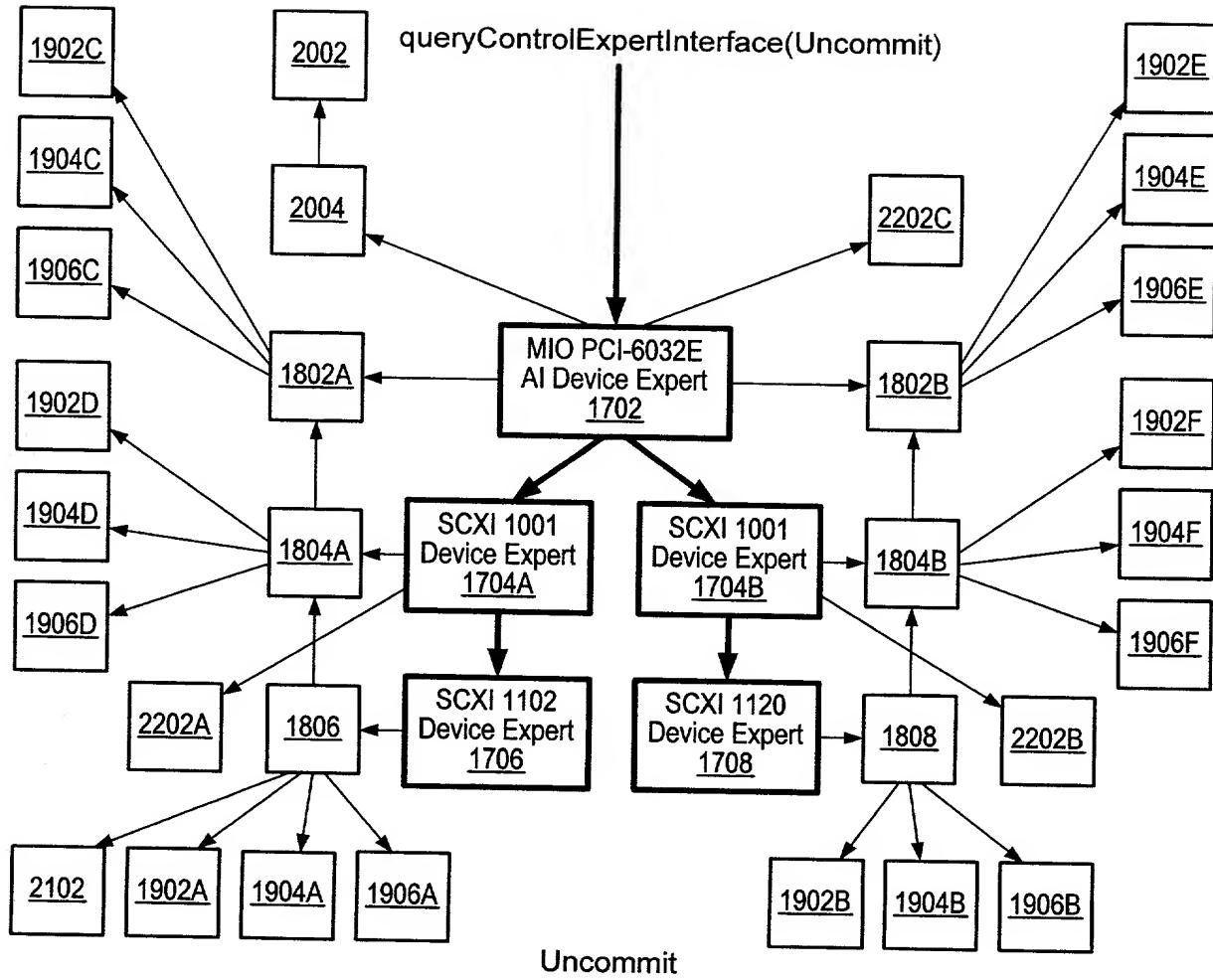
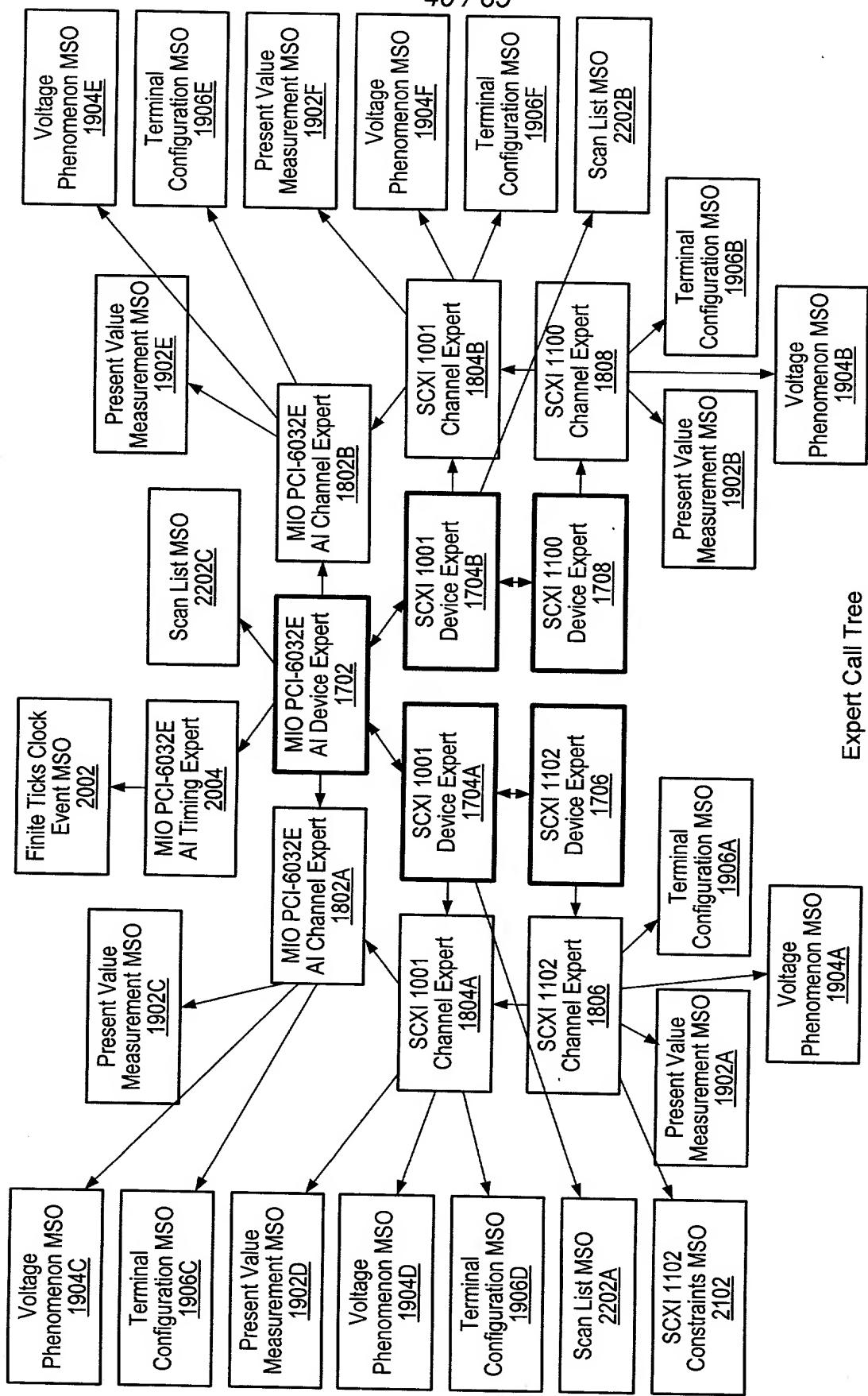


FIG. 24F



Use Case: Multi-Chassis SCXI Finite Acquisition Using An MIO

Expert Call Tree

FIG. 25

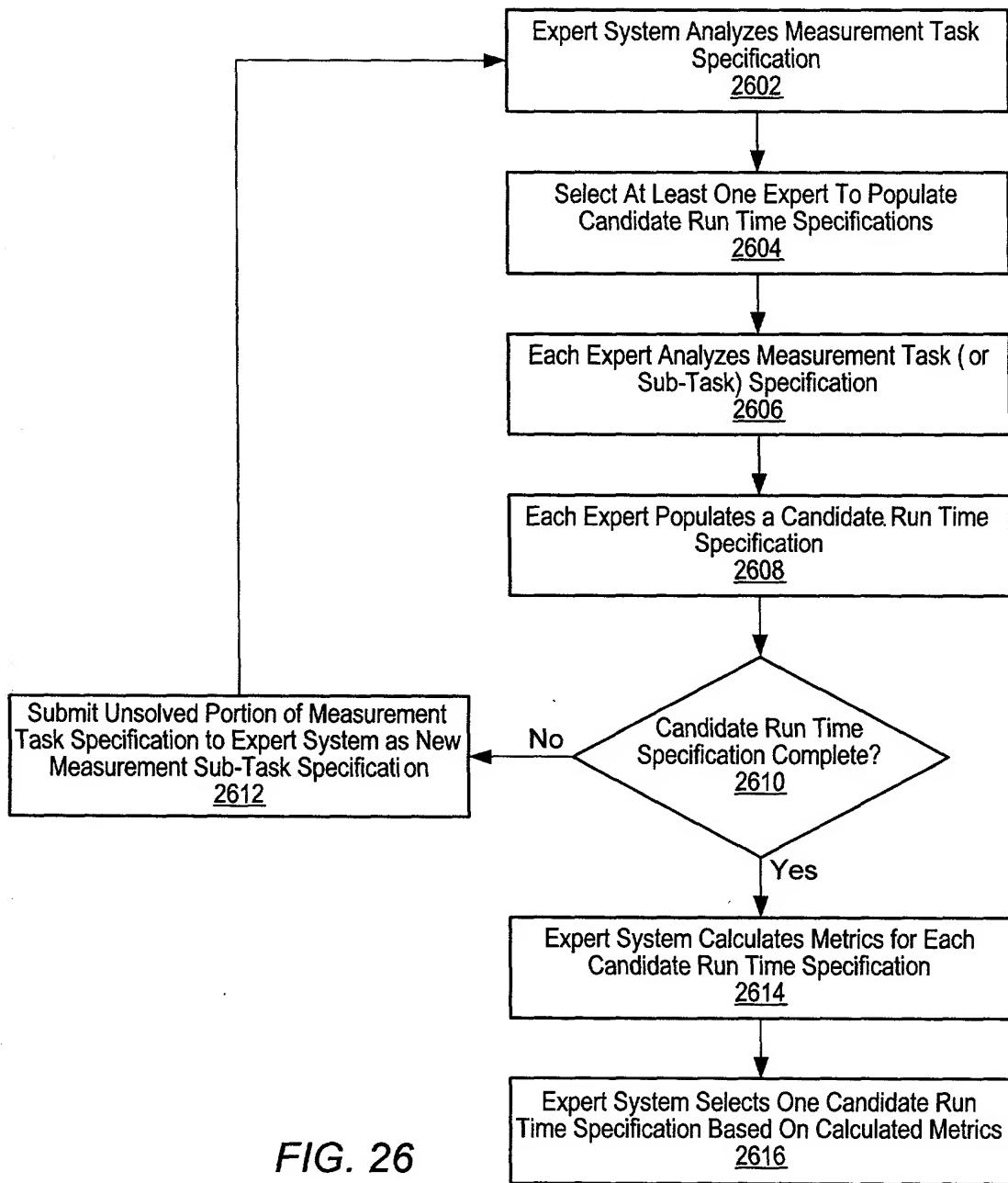


FIG. 26

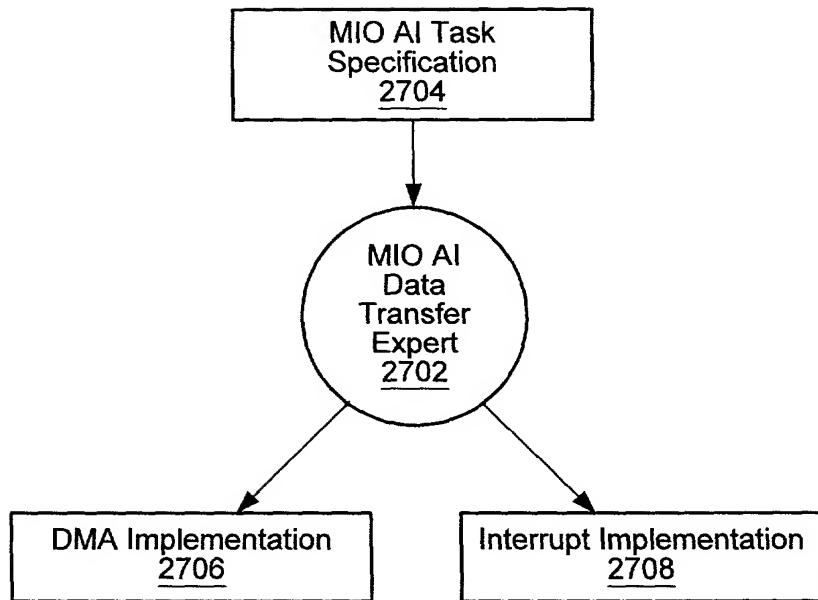


FIG. 27

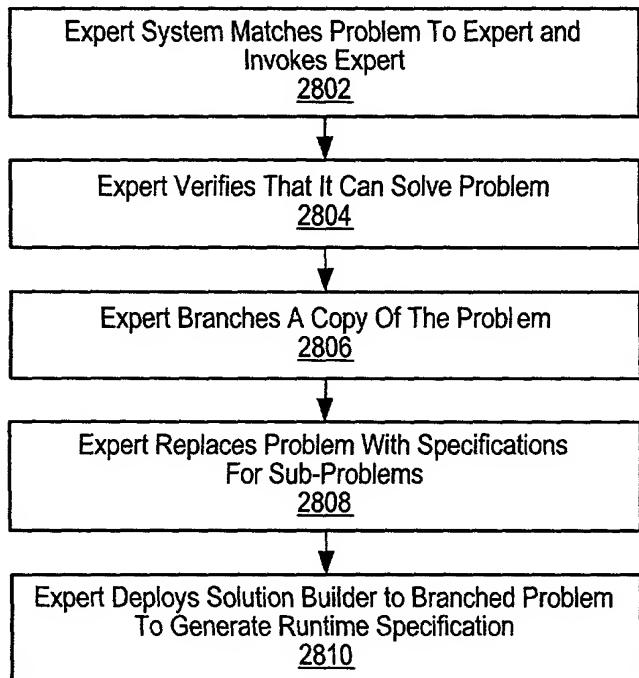
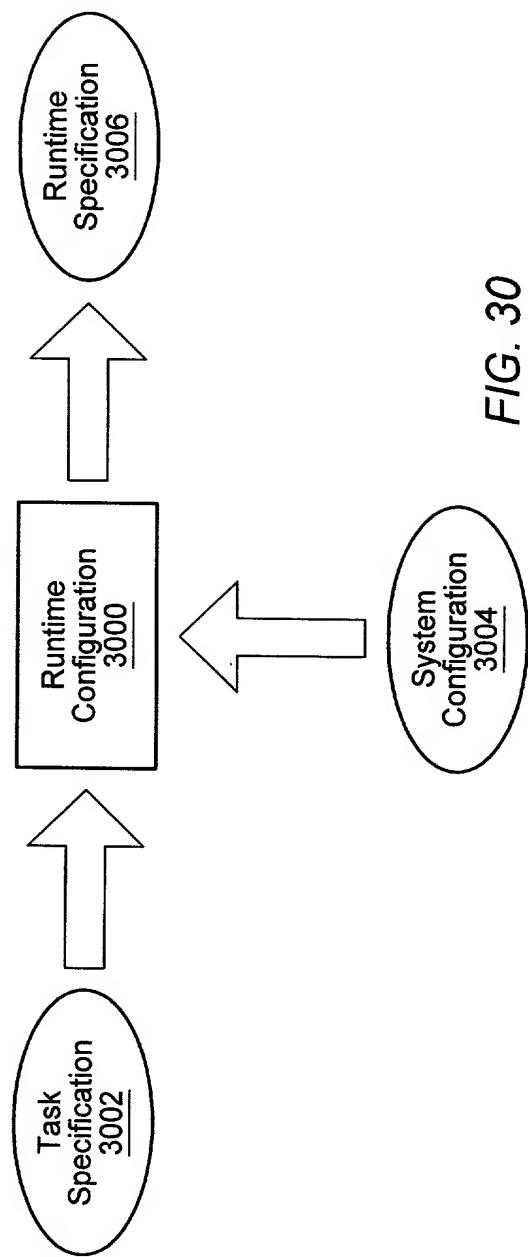
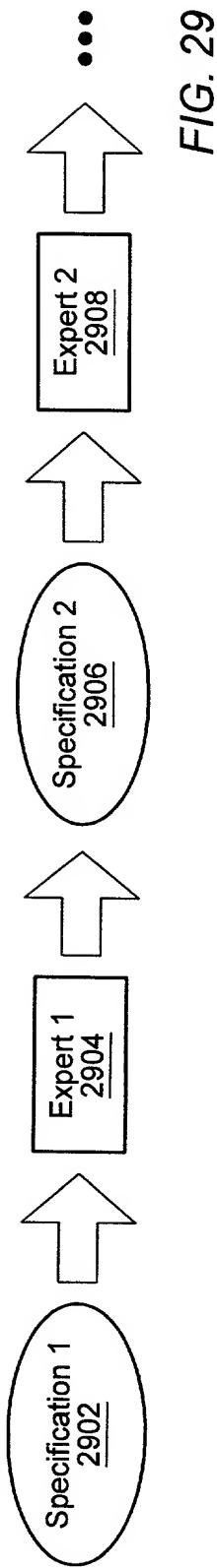


FIG. 28



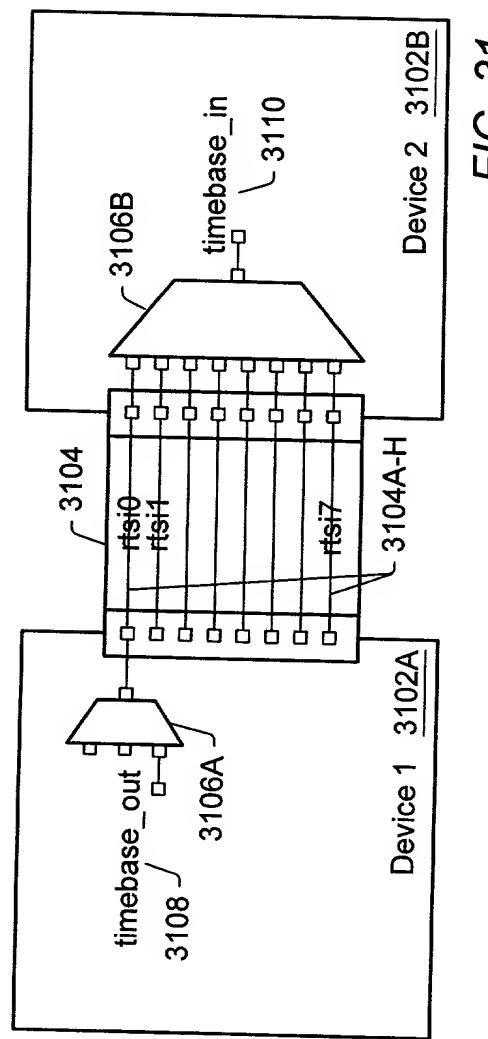


FIG. 31

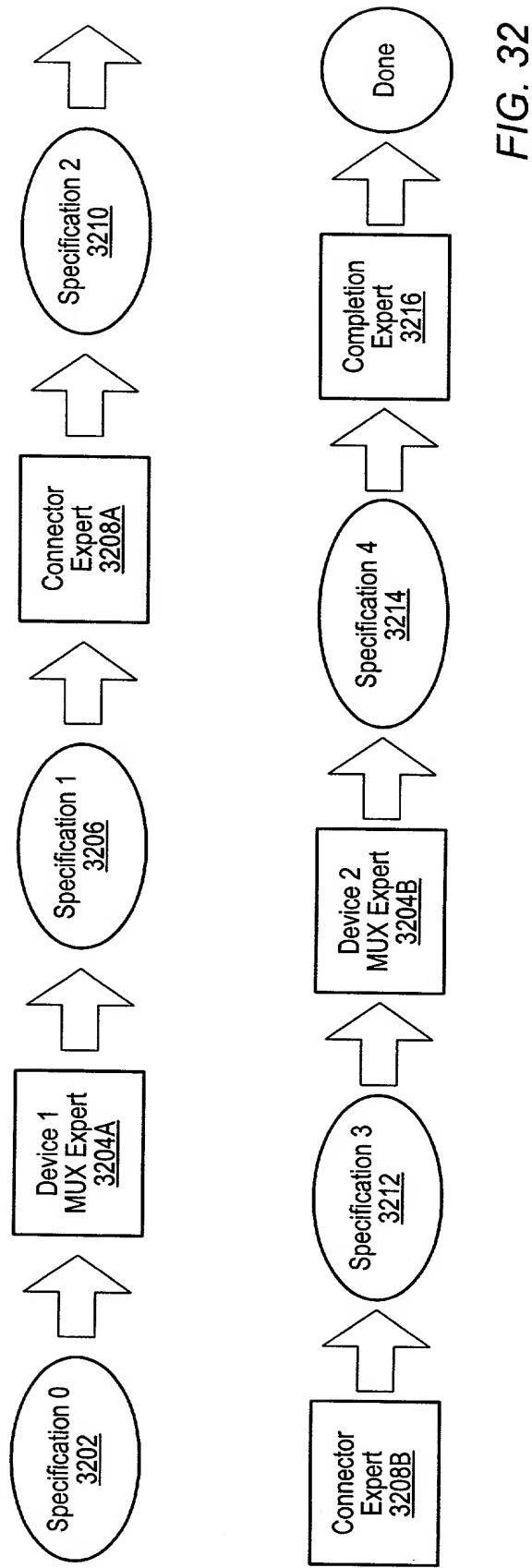


FIG. 32

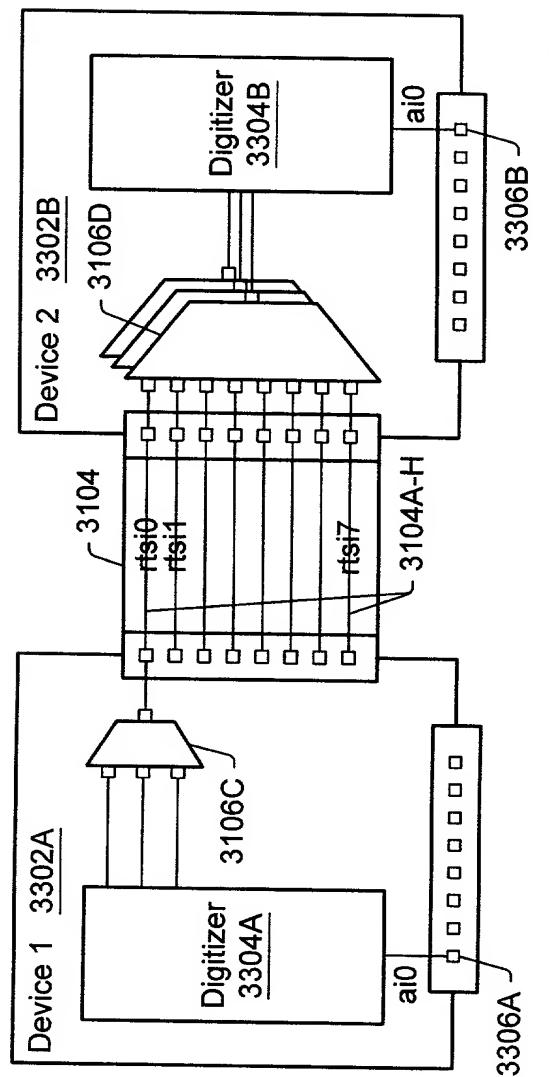


FIG. 33

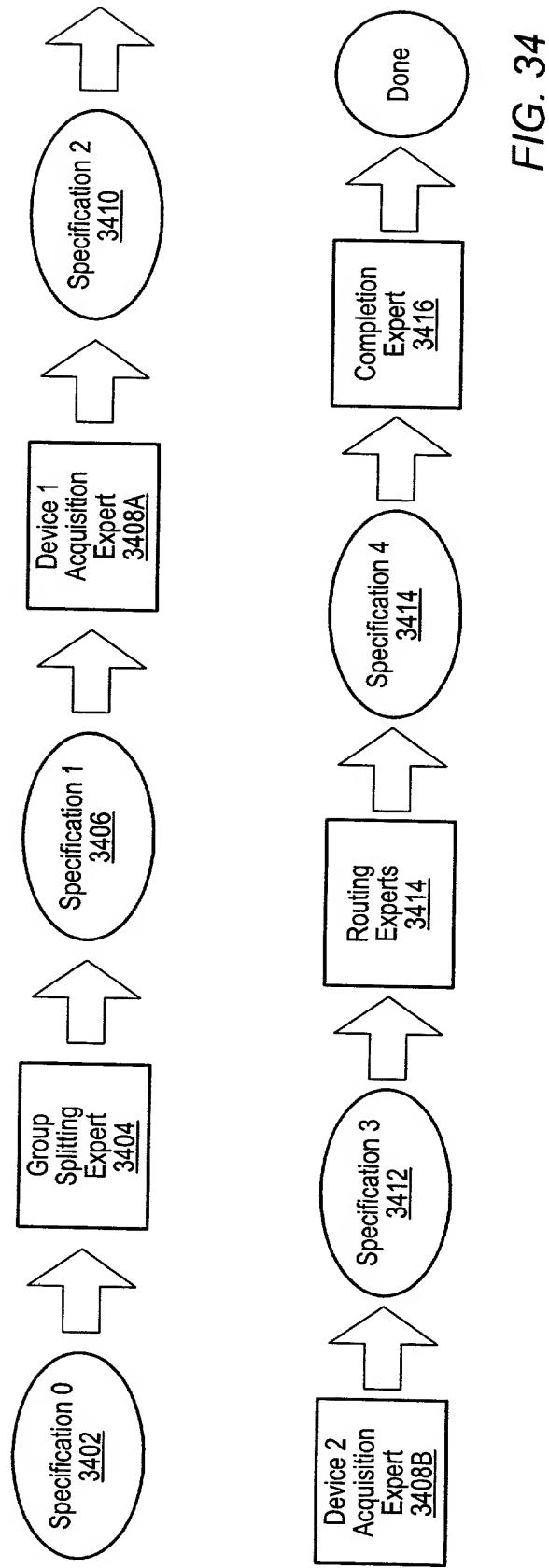


FIG. 34

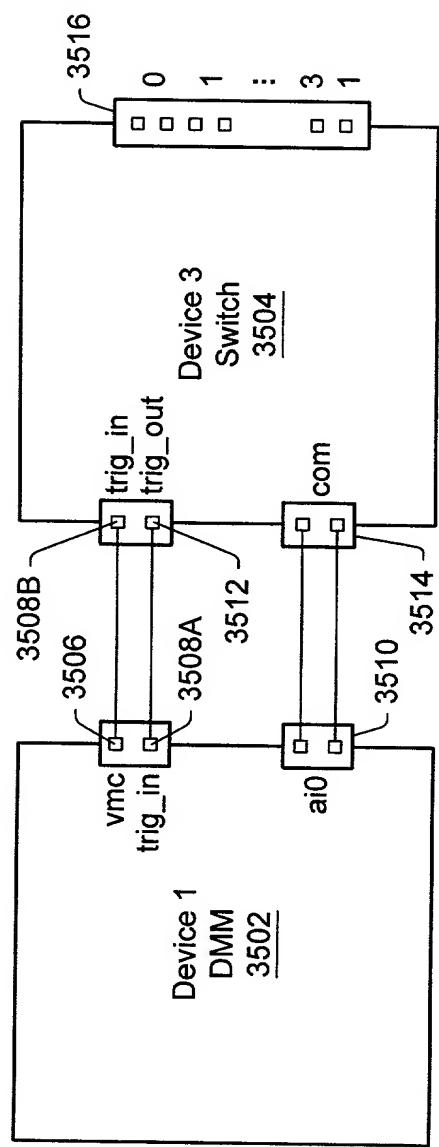


FIG. 35

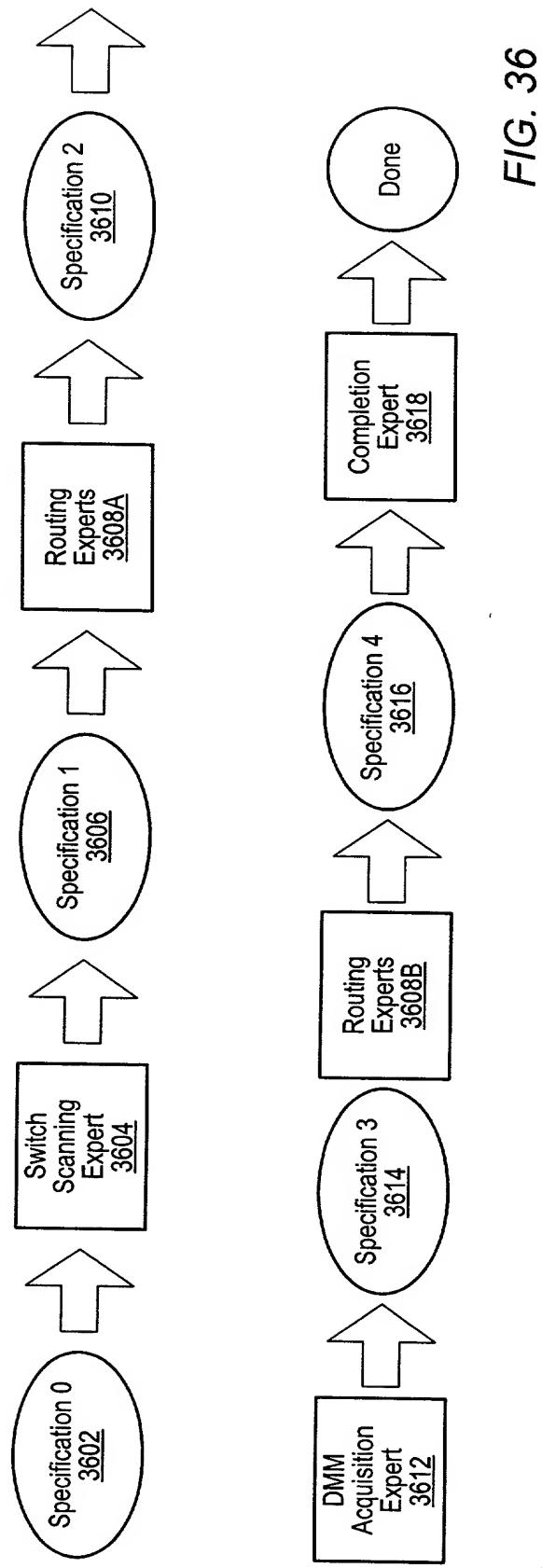


FIG. 36

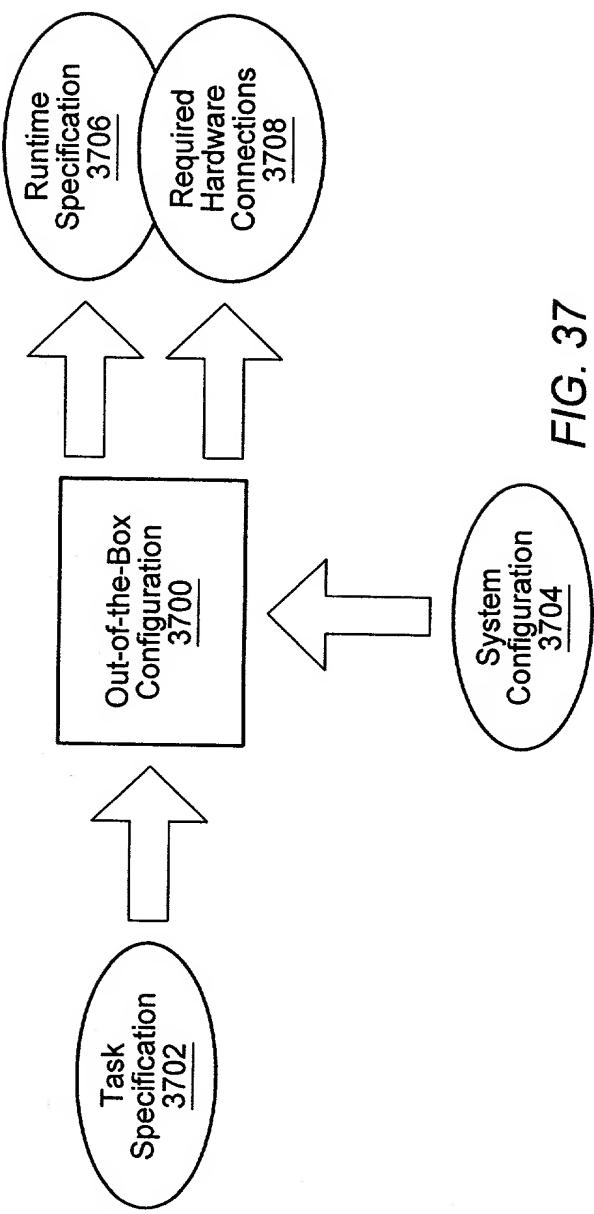


FIG. 37

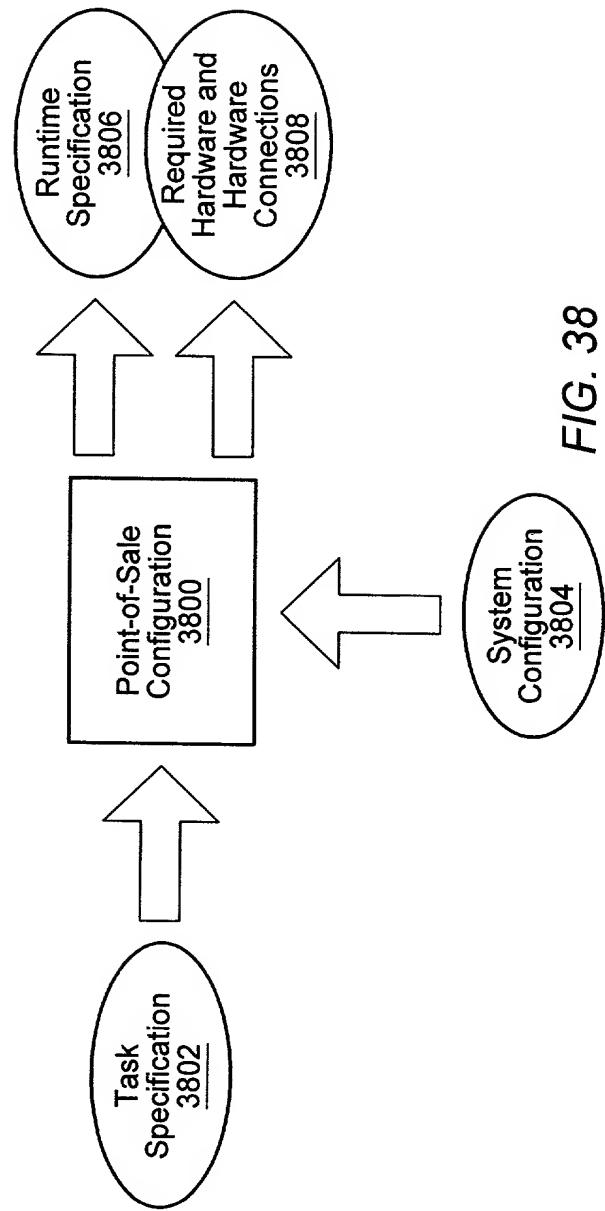
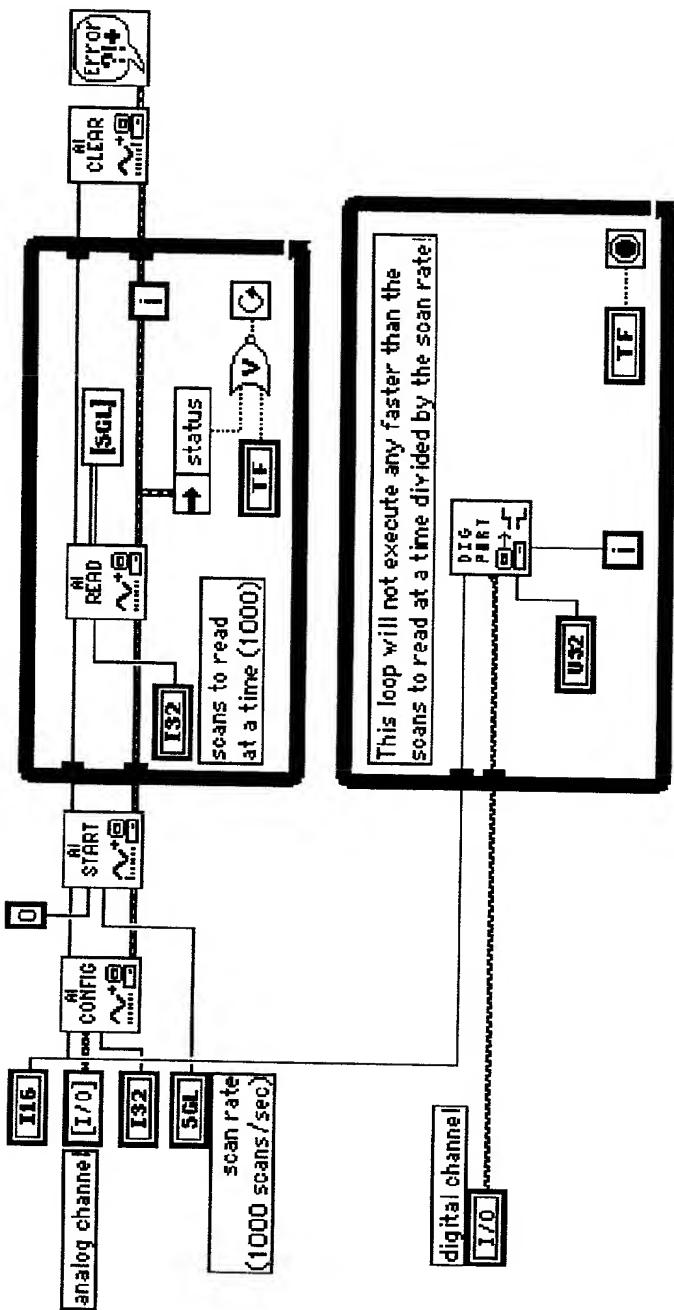


FIG. 38



**FIG. 39A**  
*(Prior Art)*

Simultaneous Buffered Analog Input And Single Point Digital Output With Single-Threaded Driver (Prior Art)

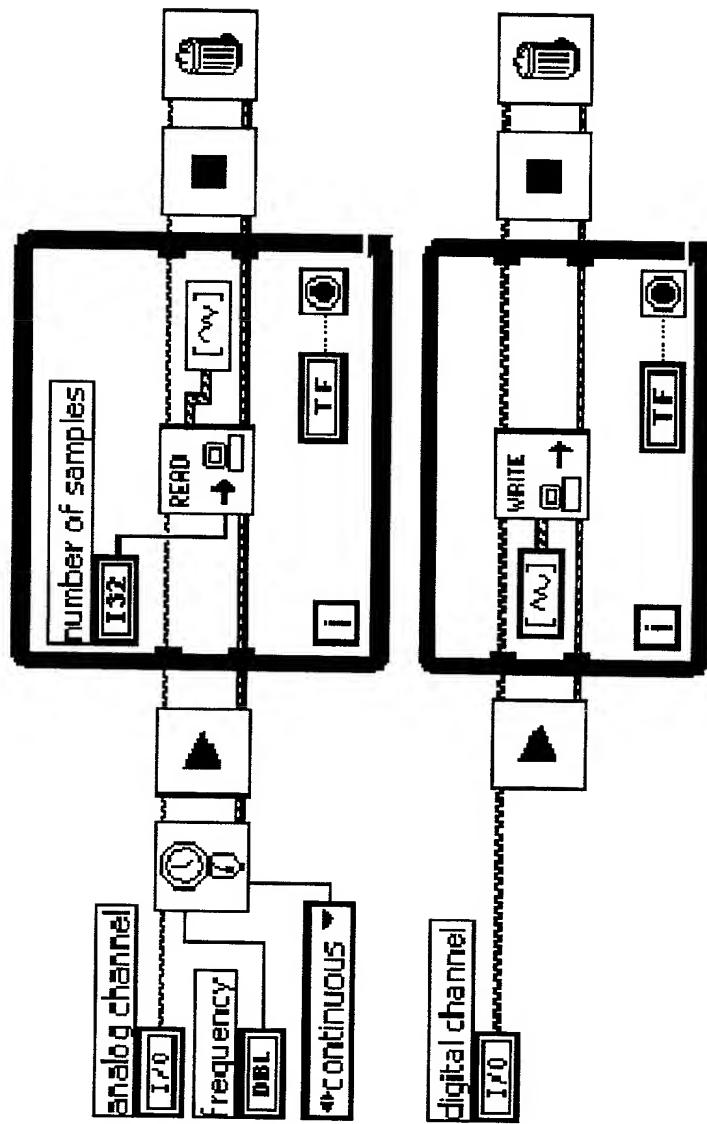


FIG. 39B  
Simultaneous Buffered Analog Input And Single Point  
Digital Output With Multi-Threaded Driver

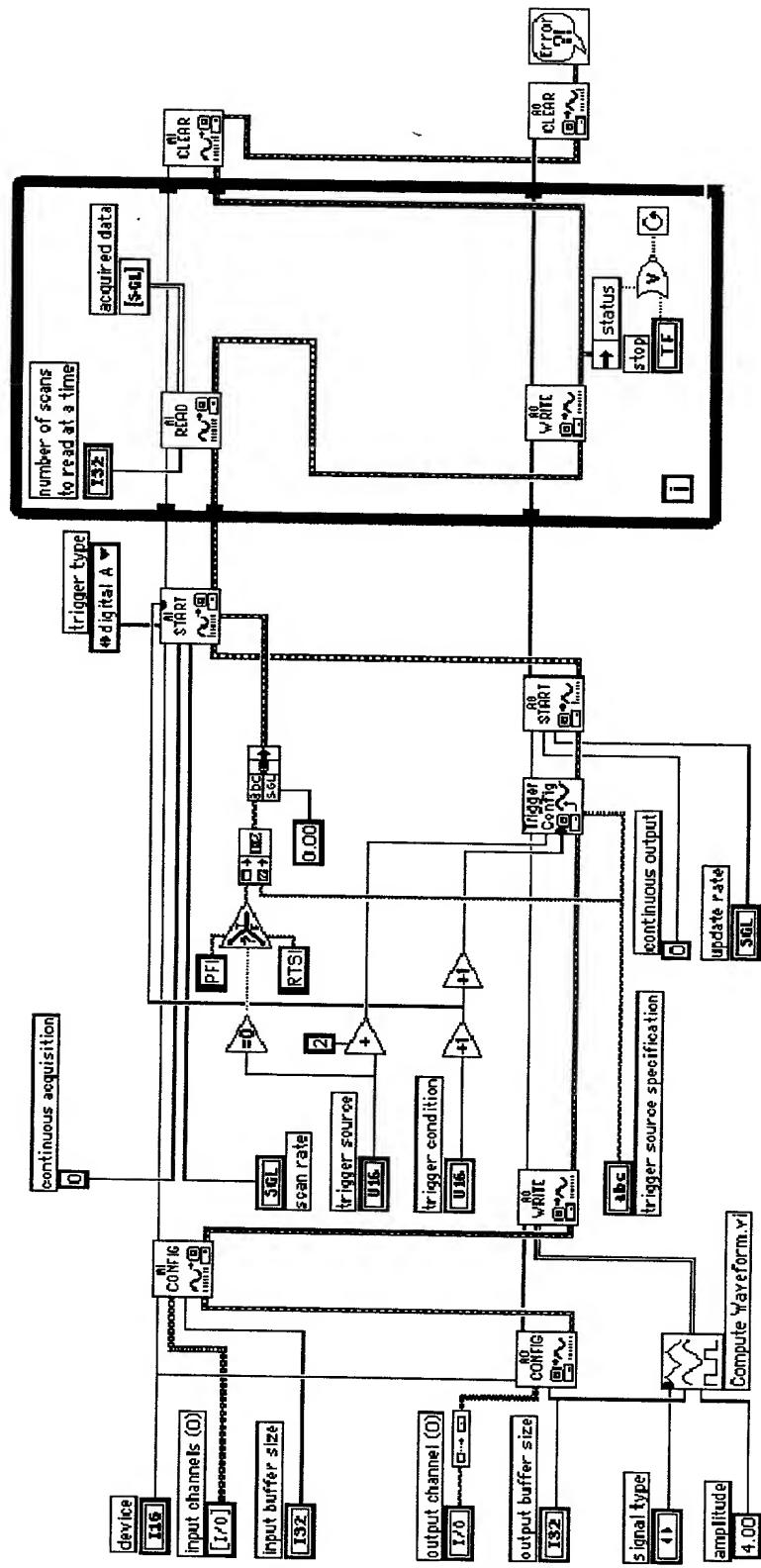


FIG. 40A

Simultaneous Triggered Buffered AI/AO (Prior Art)

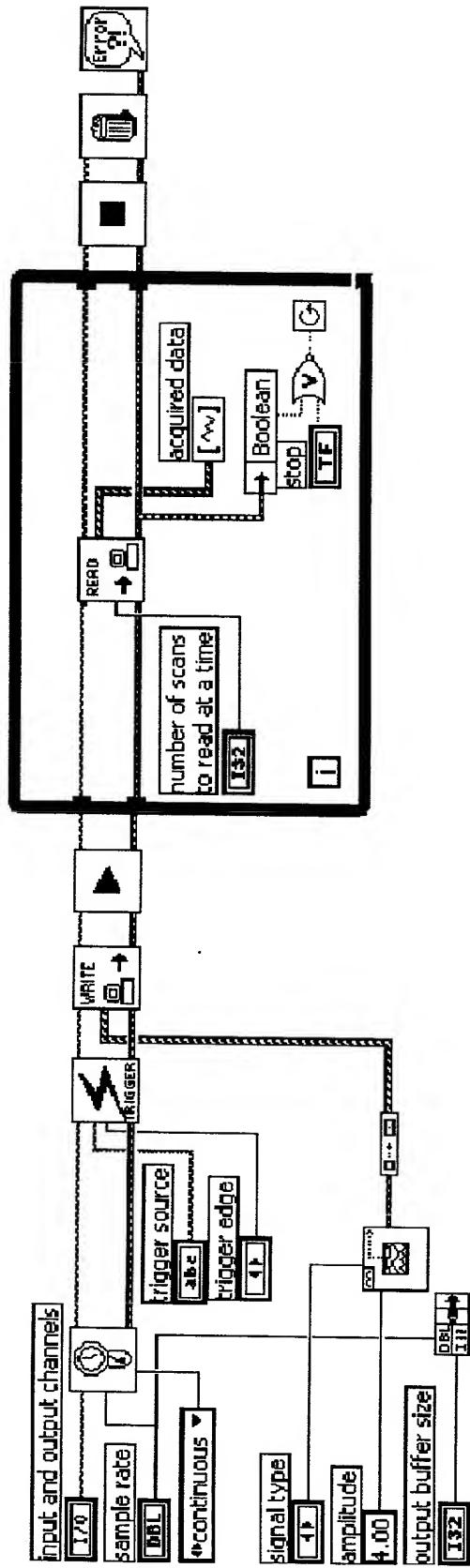


FIG. 40B

Simultaneous Triggered Buffered AI/AO

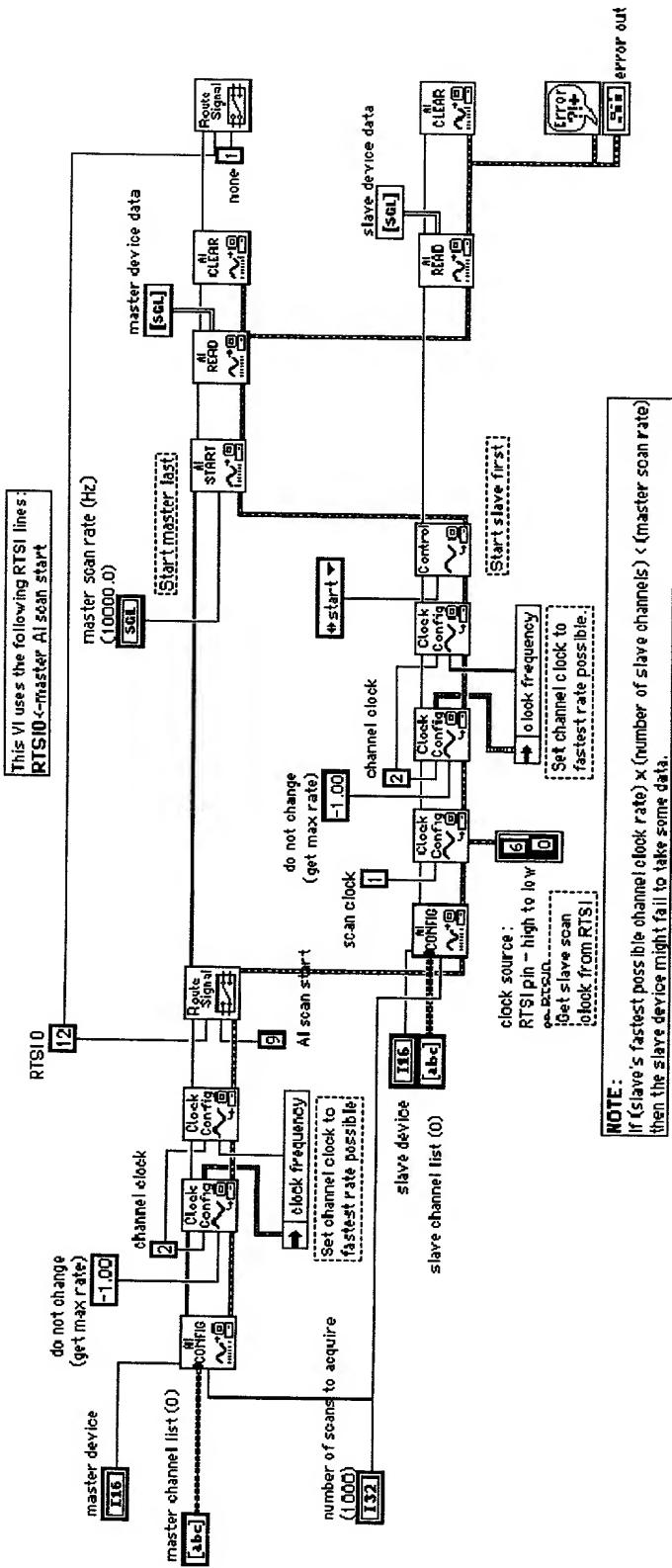
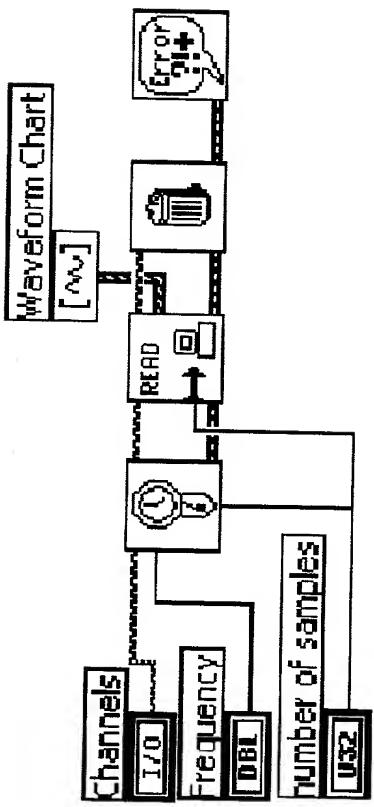


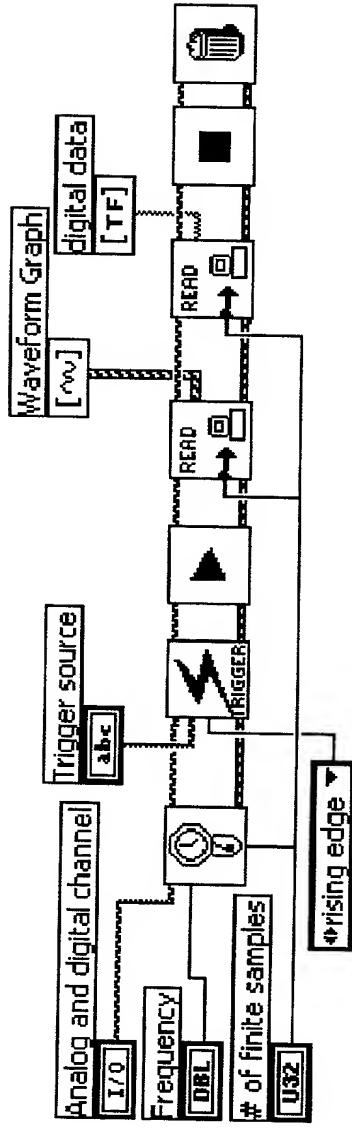
FIG. 41A

## Sharing Scan Clock Across Two E-Series Devices (Prior Art)



Sharing Scan Clock Across Two E-Series Devices

FIG. 41B



Sharing Clock And Trigger, Buffered AI &amp; DI

FIG. 42

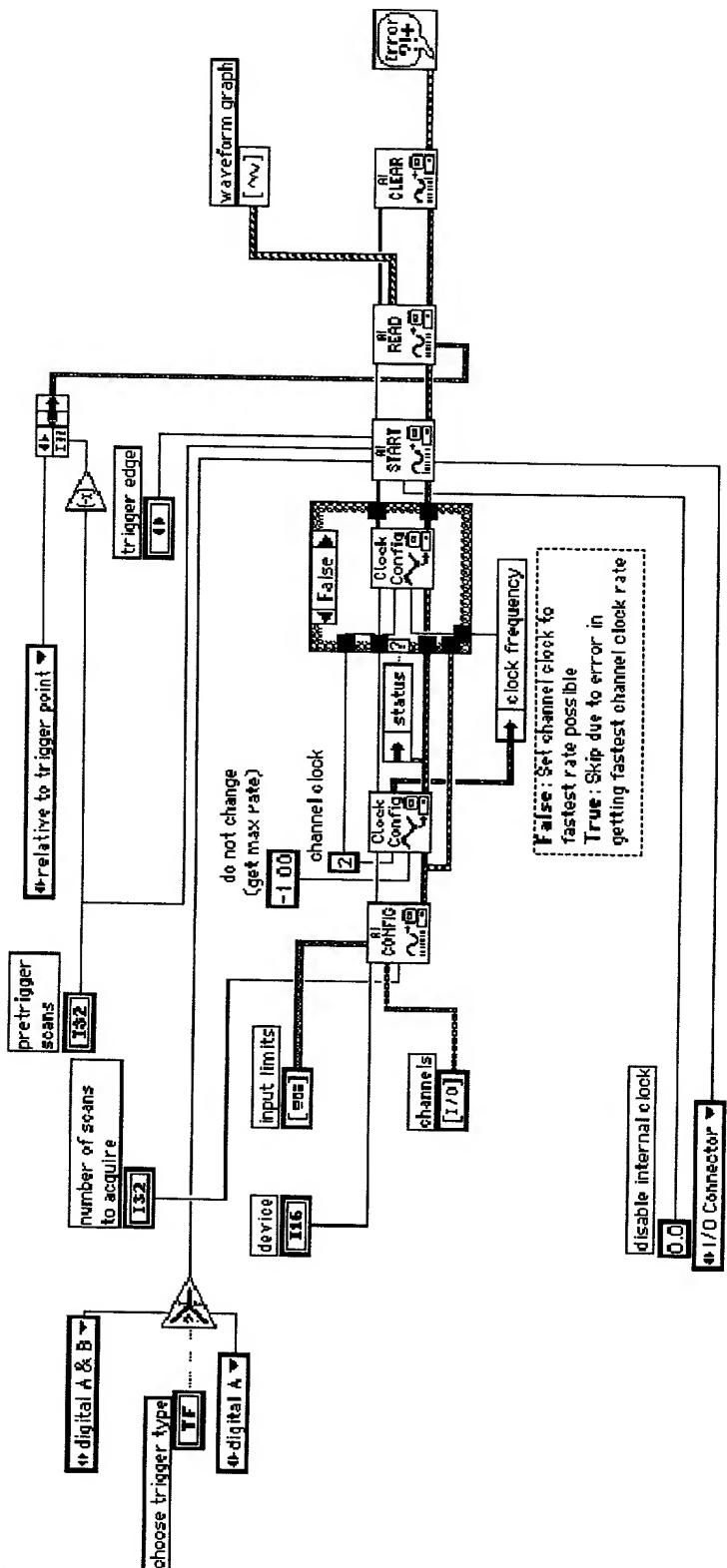


FIG. 43A  
(Prior Art)

Acquire N Scans External Scan Clock Digital Trigger (Prior Art)

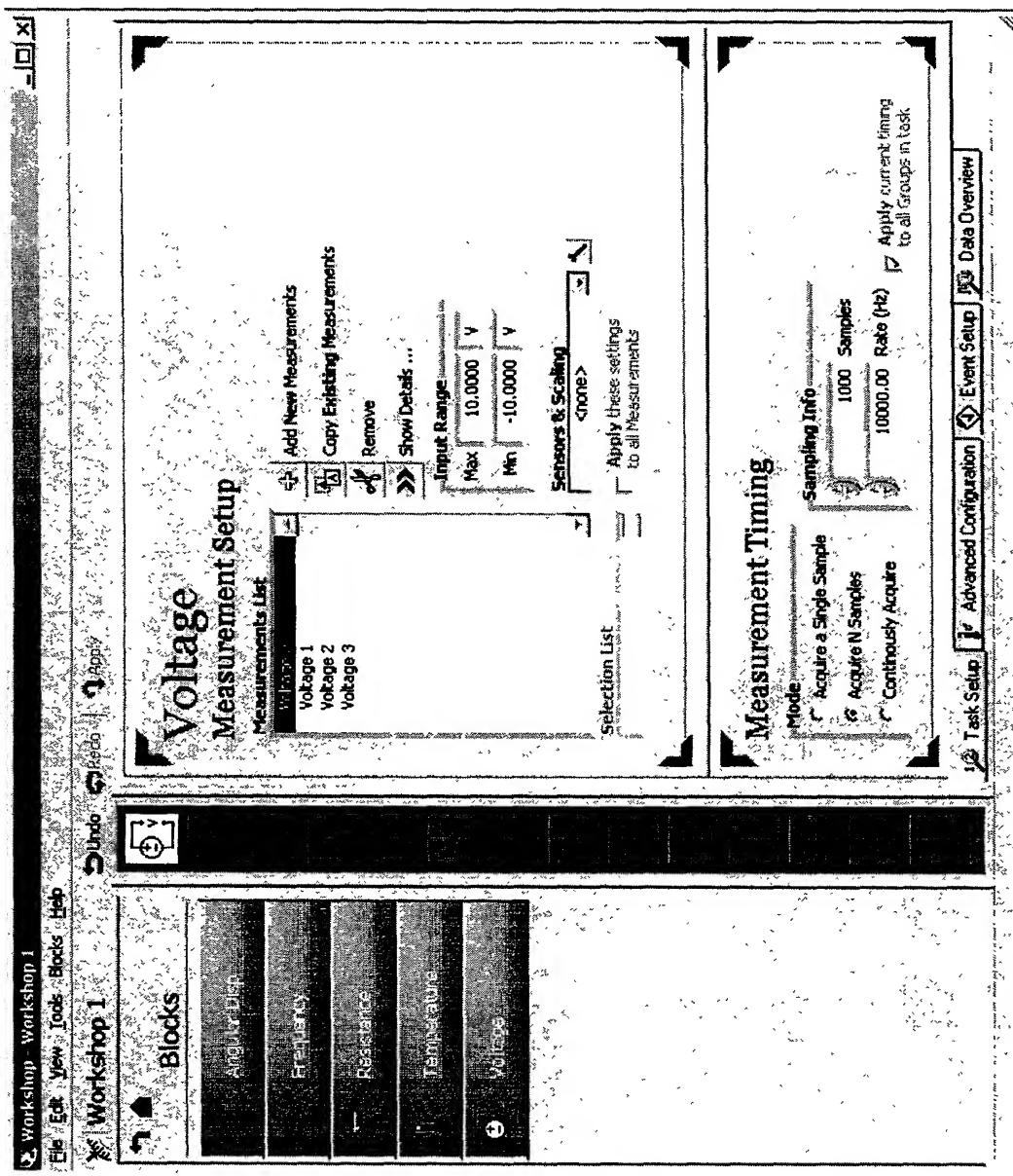


FIG. 43B

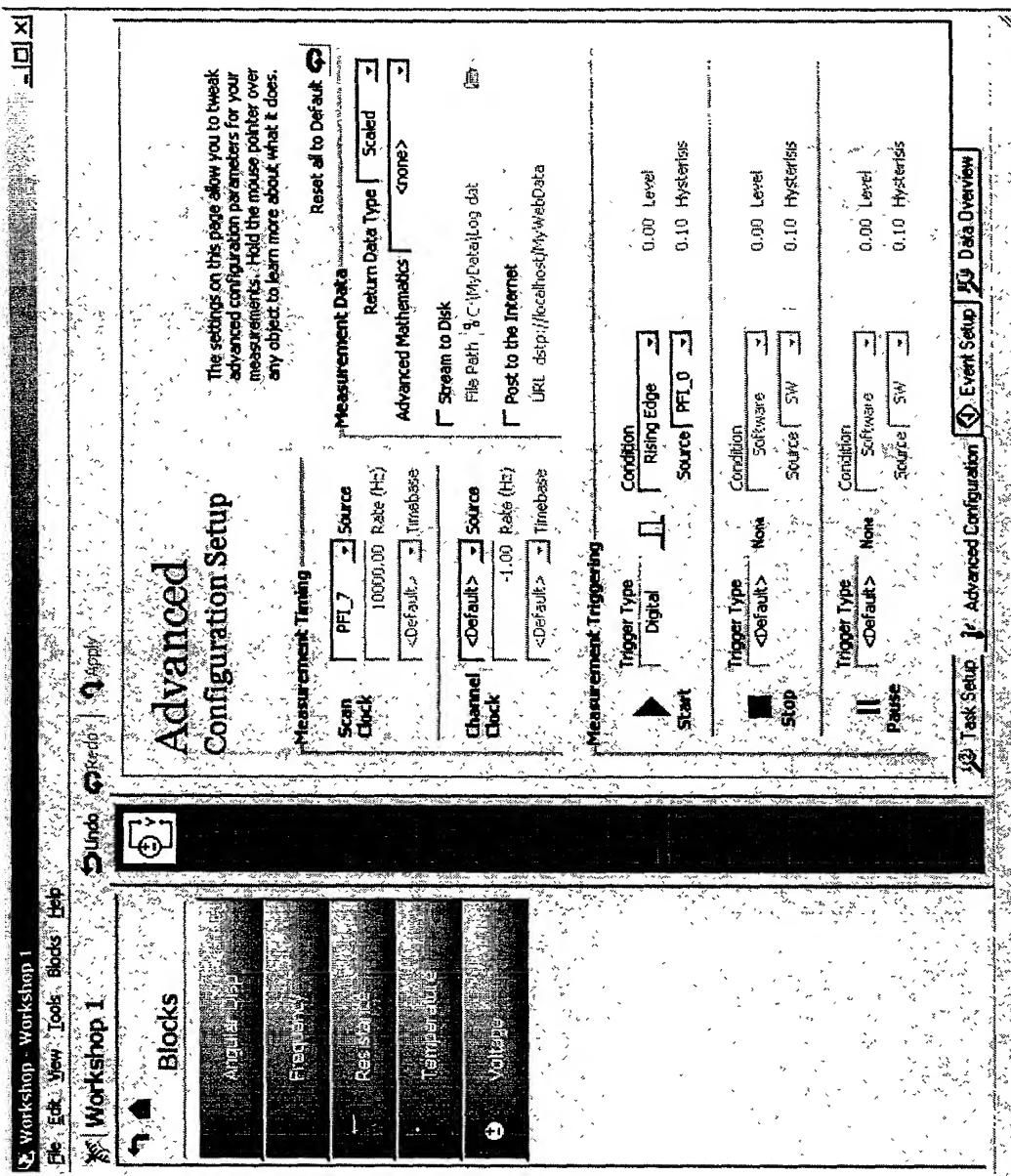
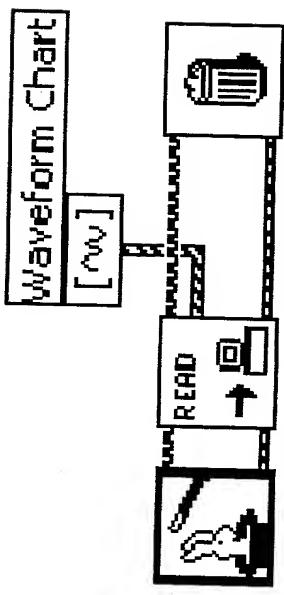
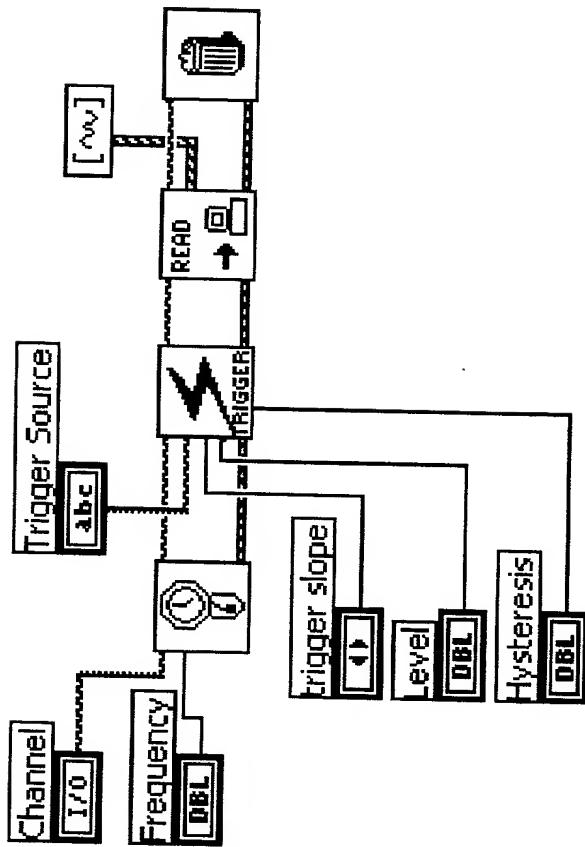


FIG. 4.3C



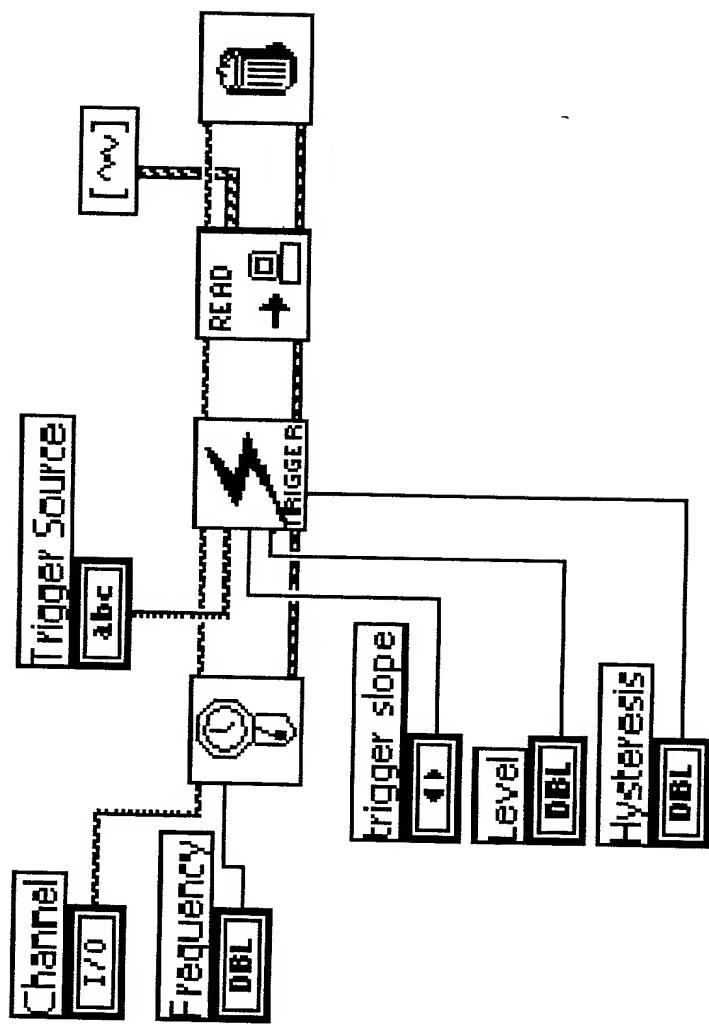
Acquire N Scans External Scan Clock Digital Trigger

FIG. 43D



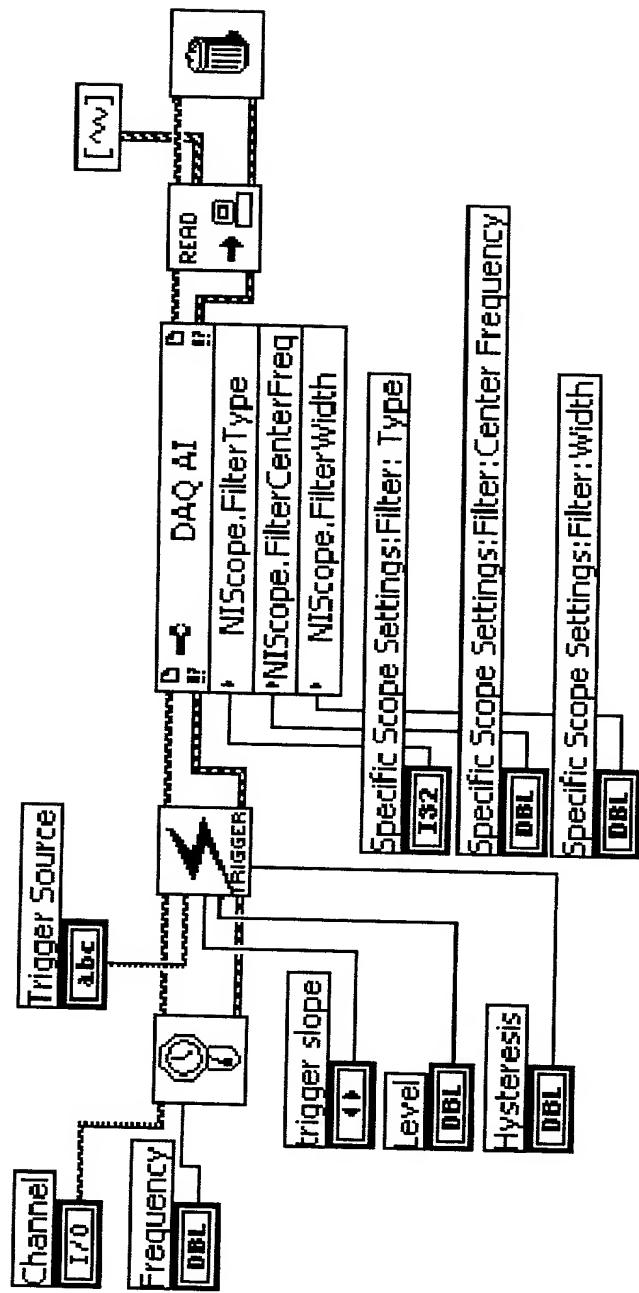
Triggered Acquisition With E-Series Device

FIG. 44A



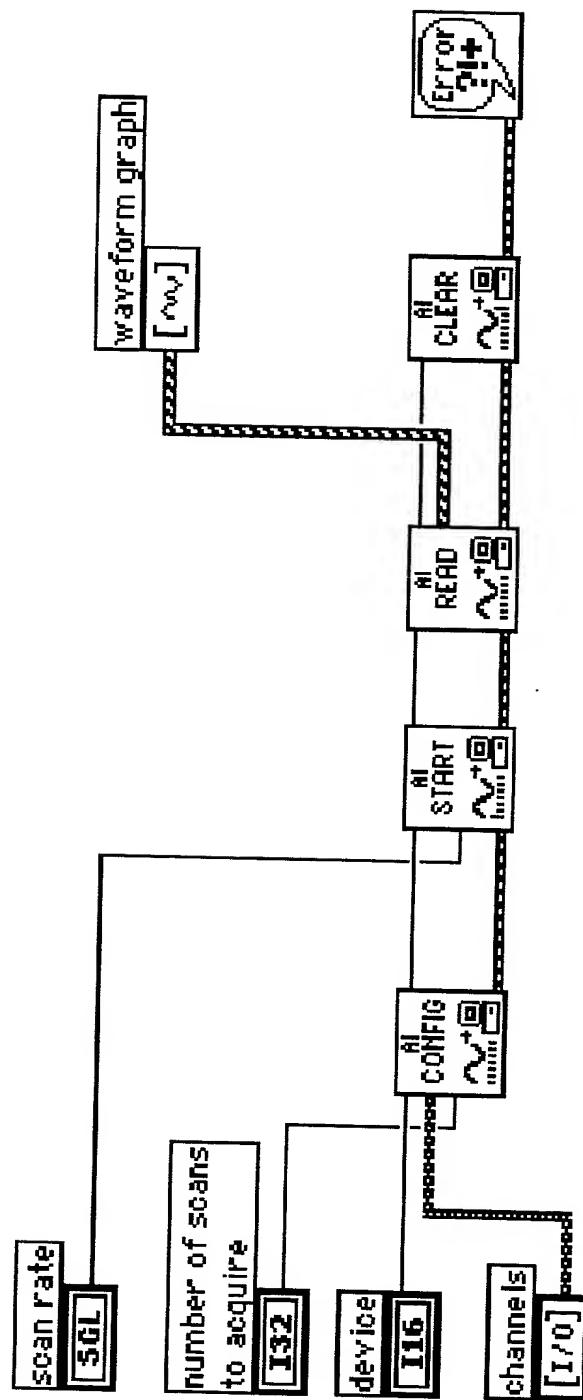
Triggered Acquisition With High Speed Digitizer

FIG. 44B



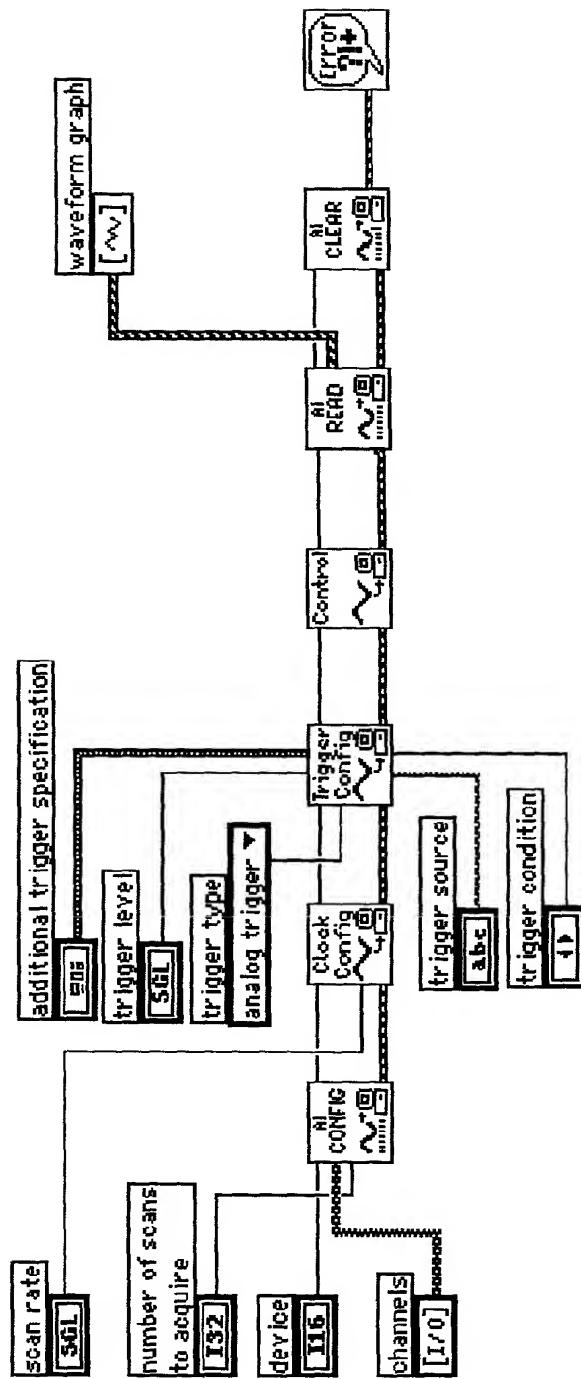
## Triggered Acquisition With High Speed Digitizer With Filtering

FIG. 44C



Intermediate Layer (Prior Art)

FIG. 45A



Changes For Analog Window Triggering (Prior Art)

FIG. 45B

